# Reconfigurable BDD based Quantum Circuits

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***Abstract*—We propose a novel binary decision diagram (BDD) based reconfigurable logic architecture based on Split-Gate quantum nanodots using III-V compound semiconductor-based quantum wells. While BDD based quantum devices architectures have already been demonstrated to be attractive for achieving ultra-low power operation, our design provides the ability to reconfigure the functionality of the logic architecture. This work proposes device and architectural innovations to support such reconfiguration. At the device level, a unique programmability feature is incorporated in our proposed nanodot devices which can operate in 3 distinct operation modes: a) active b) open and c) short mode based on the split gate bias voltages and enable functional reconfiguration. At the architectural level, we address programmability and design fabric issues involved with mapping BDD's into a reconfigurable architecture. By mapping a set of logic circuits, we demonstrate that our underlying device and architectural structure is flexible to support different functions.**
*Index Terms* **— Reconfigurability, Quantum nanodevice, Low power**

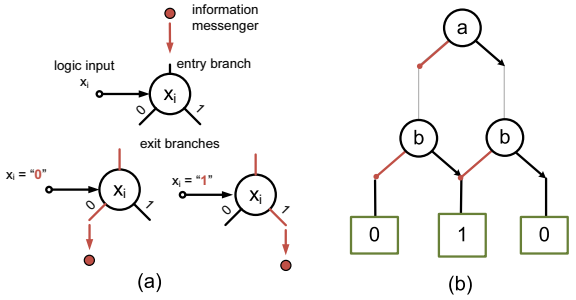


Fig. 1. A binary decision diagram (BDD) (a) node device and (b) 2 bit XOR

## I. Introduction

Technology scaling has lead to unprecedented level of integration with billions of nanotransistors on a single chip reducing cost per function. At the systems level, multi-core processor architectures aim to enhance the MIPS per watt. Still, energy consumption, device to device fluctuation and system reliability remain the primary bottlenecks to Moore's law. On the device technology front, with continued scaling, as the energy delay product approaches the fundamental quantum limit of Planck's constant, a plethora of new device concepts, charge and non charge based, have been proposed that exploit quantum phenomena as the basis of their switching operation. However, a majority of these ultra-low power emerging nanodevices operate in the single or few electron regime, thereby suffering from low transconductance, degraded output resistance and often a lack of complementary solution making it essential to co-explore emerging device design in conjunction with non-CMOS logic architecture.

Based on such co-exploration, a novel binary decision diagram (BDD) based logic architecture was proposed in [1] as a suitable candidate for implementing logic using emerging ultra-low power nanodevices. Traditionally, BDD's have been used as a data structure in CAD tools [2], [3], [4]. A BDD is a directed graph and an alternate representation of the truth table [5], [6]. Any combinational logic can be built using BDD. At every decision node the input variable determines which edge of the two edges (left or right) is active. In [7], the BDD of a combinational circuit is mapped onto a hexagonal nanowire network controlled by Schottky wrap gates.

Logic functionality is achieved by a passive path switching of messenger electrons arriving at the root node through either the left arm ("0") or right arm ("1") using the control gate of the wrap gates. Each row of the hexagonal fabric is controlled by a single variable. Both the normal and the complement of the variable are supplied to a node of the BDD and are used to control the left and right edges. A BDD implementation can be mapped onto this fabric and the variables implementing the given function establish a path in this fabric from the root (output) node to either a one-terminal or a zero-terminal to realize desired functionality (as shown in the Figure 1(b)). An input vector corresponds to a unique path from the root of the BDD to the output terminal called the conducting path (on-path). There is a current detector at the root associated to every output bit that measures the current (if any). Depending on the operating mode (active high or active low) the current flowing is interpreted as a logic one or a zero (In the active high mode, no current is a logic zero and presence of current is a logic one and vice-versa in the active low mode).

Since the path switching operation at the decision node is realized by "passive" transmission of messenger electrons through one of the arms, this implementation operates at ultra small power without requiring any large voltage gain or precise input output voltage matching or large current drivability of the node devices. Consequently, the proposed architecture produces a) lower device count than conventional Boolean CMOS logic, b) reduces wiring related energy loss, c) maintains logic functionality under millivolt supply voltage

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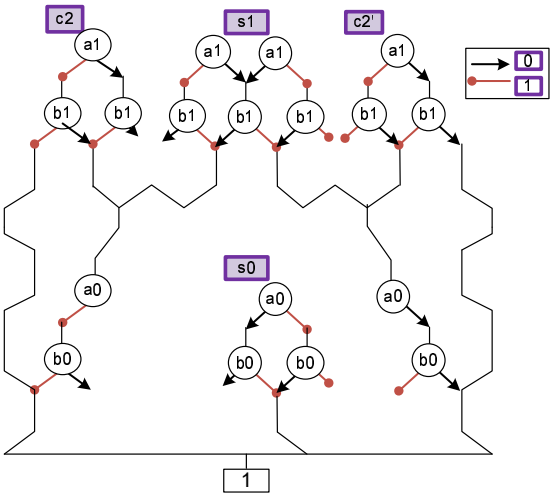


Fig. 2. Custom BDD realization of a 2-bit adder. Only edges have split gates. Missing edges of the hexagon are physically etched. Solid lines are nanowires with no split gates

with minimal or no noise margin penalty, d) operates with ultra-low power-delay product. However, the existing realization of the BDD architecture is fixed and not amenable to functional reconfiguration. Figure 2 shows a custom (non-reconfigurable) implementation of a 2-bit adder using the BDD fabric [1]. This approach selectively etches all paths that do not lead to a 1 terminal and also customizes the edges of the hexagon to either be a conducting nanowire or have a wrapped gate. Consequently, this structure is not very regular and cannot be restructured to implement a different function due to the physical etching process involved in its realization. Furthermore, if any of the nanowire segments or the wrap gates is defective, the whole circuit becomes non-functional. This is a significant limitation considering that nanowires and few electron quantum nano-devices have traditionally suffered from variability and reliability issues. Consequently, this work proposes a novel binary decision diagram (BDD) based reconfigurable logic architecture.

The specific contributions of this paper are:

1) We propose a novel binary decision diagram (BDD) based reconfigurable logic architecture based on Split-Gate quantum nanodots using III-V compound semiconductor-based quantum wells. We incorporate a unique programmability feature in our proposed nanodot devices which can operate in 3 distinct operation modes: a) active b) open and c) short mode based on the split gate bias voltages and enable functional reconfiguration.
2) We address programmability and design issues involved with mapping BDD's into a reconfigurable architecture. We quantify the additional overheads in mapping design on to the reconfigurable fabric for a set of applications. Our results indicate that our underlying device and architectural programmability is flexible enough to support low overhead reconfiguration.

The rest of the paper is organized as follows. Section 2 explains the device structure required to support our reconfigurability. Section 3 discusses the architectural and mapping issues related to reconfiguration. Section 4 discusses related work. Section 5 provides conclusions.

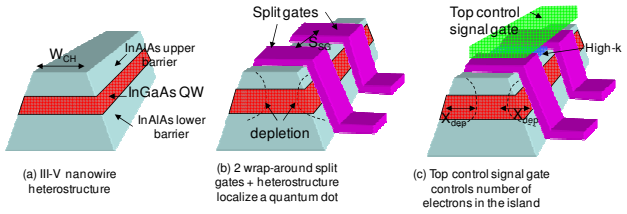


Fig. 3. Schematic illustrating the a) III-V nanowire formation b) wrap-around Schottky split gate formation c) top control gate formation

## II. Reconfigurable Device Structure

In our binary decision diagram circuit, we incorporate new functionality by utilizing the reconfigurability feature of our proposed device via additional gate input, $V_{SG}$, controlling the sidewall depletion and the tunneling barrier.

### A. Reconfigurable device structure

While the former approaches have been successful in demonstrating single electron tunneling behavior with stable and reproducible Coulomb oscillations, our approach aims at incorporating reconfigurability feature into the device using bias dependent modulation of the tunnel barriers. The basic architecture of the proposed device is shown in Figure 3.

First, an InP-based quantum-well heterostructure grown using solid-source MBE technique (molecular beam) is patterned into nanowires of width $W_{CH}$. A pair of wrap-around Schottky gates around the nanowire called split gates is defined using e-beam evaporation and liftoff technique. The separation between the split gates, $S_{SG}$, to first order, will control the size of the dot and the energy separation of the quantized levels. The depletion region induced by the electrostatic action of the split gates forms the double tunneling barriers at the source and drain ends while the quantum-well heterostructure provides the vertical confinement. Together, they isolate the quantum dot between the source and drain tunnel junctions whose barrier height and width as well as the dot size are controlled using the bias, $V_{SG}$, on the split gates. The bias on the split gates provides the reconfigurability feature to the quantum dot enabling it to operate in three different modes: active, open and short. There is also a top control gate, $V_{CG}$, separated from the quantum dot and the split gates via a deposited high-K gate dielectric. The top control gate, $V_{CG}$, controls the dot potential independently once the transistor is biased into active mode and is used as the input control signal electrode to allow or block the node electrons to tunnel through the island. The device parameters can be estimated, to the first order, based on the following simple formulae:

$$C_{cg} = \frac{\epsilon_{High-K} * W_{CH} * S_{SG} * \alpha}{T_{High-K}} \quad (1)$$

$$C_s, C_d = \frac{\epsilon_{InGaAs} * W_{CH} * X_{dep}(V_{SG}) * \beta}{W_{SG}} \quad (2)$$

where $C_{cg}$ is the capacitance between the control signal gate and the island, $C_s$ and $C_d$ are source/drain tunnel junction

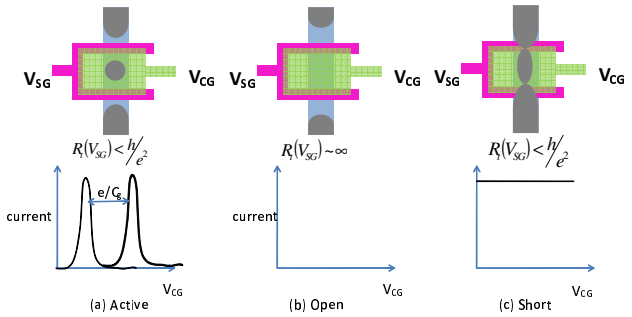


Fig. 4. Various modes of operation of the split gate nanodot device controlled by the wrap-around Schottky gate.

capacitances, $X_{dep}(V_{SG})$ is a depletion layer depth set by the bias $V_{SG}$, $\alpha$ is the size shrinkage factor of the electrically formed island, $\beta$ is the size shrinkage factor of the electrically induced tunnel junction directly controlled by $V_{SG}$ and $W_{SG}$ width of the sidewall split gates.

From the viewpoint of a reconfigurable device structure, a strong coupling between the side depletion gate (split gate) and the III-V nanowire as well as a strong coupling between the control gate and the island is desirable. The Schottky wrap-around gate feature for the split gates satisfies the former requirement whereas the high-k dielectric between the control gate and the top nanowire surface ensures the latter. The split gate bias, $V_{SG}$, is used to set the single electron device in 3 unique modes of operation: a) Active b) Open and c) Short. Figure 4 assumes that the $V_{SG}$ potential is applied to some universal ground potential.

In order to provide a local reference bias, we modify the split gates as shown in Figure 5(a) and apply the $V_{SG}$ across the terminals $V_{SG1}$ and $V_{SG2}$. This modifies the device structure to have the top portion of the wrap-gate to be removed leaving the two sidewalls with independent voltage control. This is the central feature of our device structure which will be exploited later for functional reconfigurability of the BDD-based logic blocks. In the active mode, the split gate bias, $V_{SG}$, is first adjusted to make the tunneling resistance of the source and drain junctions to exceed the resistance quantum, $h/e^2$, but still low enough to allow efficient tunneling (Figure 4(a)). This condition is necessary to suppress the quantum fluctuations in the electron number, n, of the quantum dot so that the electronic charge on the island is well localized. Then the control bias, $V_{CG}$, and its complement signal will control the dot potential to block or allow single/few electron tunneling.

In the open mode, $V_{SG}$, is set to a sufficiently negative value to allow the depletion regions from both sides to encroach and deplete off the nanodot island completely, resulting in an electrically equivalent open circuit (Figure 4(b)). Finally, in the short mode, a large positive $V_{SG}$ is applied so that the tunnel junctions become almost transparent and the tunneling resistance is significantly reduced below the resistance quantum, $h/e^2$. In such a mode, the Coulomb blockade behavior of the nanodot is removed and the device behaves like a near ohmic conductor. (Figure 4(c)). In contrast to previous works on single electron transistors, our device structure has the unique

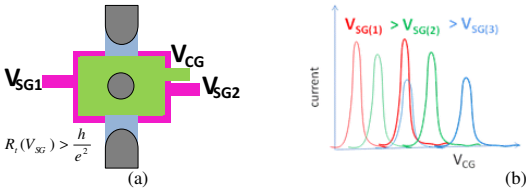


Fig. 5. (a) Split gate bias applied across $V_{SG1}$ and $V_{SG2}$ and (b) Split gate bias dependence of the nanodot I-V characteristics. The position as well as peak current are modulated by $V_{SG}$

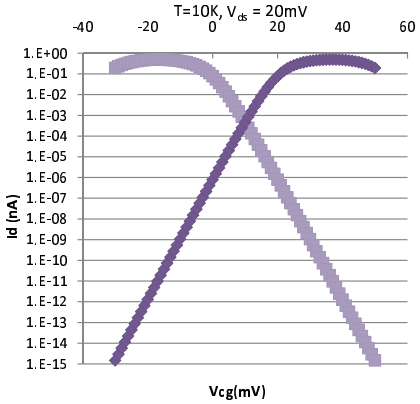


Fig. 6. $I_d$ vs $V_{CG}$ characteristics under active mode($I_d$ is log scale)

feature in that the sidewall depletion gate can deterministically control the functionality of the single electron transistor useful for implementing reconfigurable logic architectures as described later.

The split gate bias also allows additional functionality to control the peak current position, peak to valley ratio as well as the spacing between the peaks. Figure 5(b) shows that as $V_{SG}$ is decreased towards negative values (red to green to blue), the depletion region widens, increasing the tunneling barrier resistance and decreasing the peak tunneling current. And the modulation of the peak position originates from the sharing of the island charge between the top control gate and the split gates. This additional control of the position of the Coulomb oscillation peak to control the leakage issues at the decision nodes and investigate the tradeoffs thereof. This capability allows us to modulate the precise positioning of the Coulomb peaks in the devices and address fabrication tolerances: a) dot size fluctuation from split gate spacing variation b) split gate length variation c) nanowire width variation as well as d) device aging.

### B. Device Model

We model the quantum device using the steady-state master equations proposed by [8].

$$\begin{aligned} f(x) &= x\sinh\left(\frac{x}{\tilde{T}}\right) \\ G &= \frac{\tilde{V}_{CG,n}^2 - \tilde{V}_{DS}^2}{f(\tilde{V}_{CG,n}) - f(\tilde{V}_{DS})} \\ I_d &= \frac{e}{2R_\Sigma C_\Sigma} G \sinh\left(\frac{\tilde{V}_{DS}}{\tilde{T}}\right) \end{aligned} \tag{3}$$

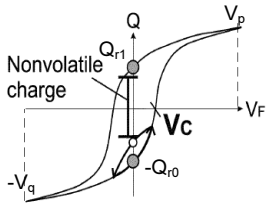


Fig. 7. Non-volatile charge in a ferroelectric capacitor

$$
\begin{aligned}
H &= \frac{2C_{cg}V_{CG}}{e} - \frac{(C_{cg}+C_s-C_d).V_{DS}}{e} \\
\tilde{V}_{CG,n} &= H - 1 - 2n \quad (4) \\
\tilde{V}_{DS} &= \frac{C_\Sigma V_{DS}}{e} \quad (5) \\
\tilde{T} &= \frac{2k_BTC_\Sigma}{e^2} \quad (6) \\
C_\Sigma &= C_{cg}+C_d+C_s \quad (7) \\
R_\Sigma &= R_d+R_s \quad (8)
\end{aligned}
$$

$C_{cg}$ is the capacitance between the control signal gate and the island. $C_s$ and $C_d$ are source and drain tunnel junction capacitances. $R_s$ and $R_d$ are the tunneling resistances of the source and drain tunnel junctions. Using split gate bias control for SETs has been demonstrated for silicon-on-insulator nanowire and applied for dynamic multifunctional logic [9], [10]. The $I_d$ with respect to the control gate voltage in case of active and with respect to the split gate bias for the open or short modes are plotted at a low temperature of $10K$ and $V_{DS}$ of 20mV. Figure 6 (a) shows the IV characteristics in the active mode for both the normal and complement voltages. It can be seen from the graph that the $V_{CG}$ swing required for the device functionality with an Ion/Ioff ratio of roughly $10^3$ is around 25 to 27mV. The dynamic power consumption of the device is very low and of the order of $10^{-12}W$ which is three orders of magnitude better than current MOSFETs.

The split gate bias voltage gives fine control over the tunnel resistance by widening or thinning down the width of the depletion region resulting either in an open or a short. In addition, because of the proximity of the split-gate to the tunnel barriers, it has a more powerful effect on the device than control gate. Thus, it can override the control gate. Further, the split-gate bias voltage is also in the range of 20mV yet can over rule the control gate.

### C. Non-volatility Property

We propose further modification of the Schottky split gate structure to incorporate nonvolatile feature into the devices. For example, a ferroelectric insulator could be inserted between the split gate electrode and the nanowire instead of a direct metal-semiconductor Schottky gate. The ferroelectric capacitor will store the polarization charge even when the split gate bias has been removed and retain the tunnel barrier properties of the single electron transistor (Figure 7).When a bias $V_f$ is applied across the ferroelectric capacitor, the polarization charge $Q(V_f)$ in the capacitor shows a hysteretic Q-V characteristic with a remanent polarization charge $Q_r$. This remnant charge on the split gate is capable of inducing a shift in the flat band voltage values and would modify the depletion region characteristics modulating the tunnel barrier. The device operates as a open or short structure when the polarization state is $Q_{r0}$ or $Q_{r1}$. The device operates in normal mode, when there is no remanent polarization (the intersection of the hysteresis curve with the X-axis). To program to $Q_{r1}$ $(Q_{r0})$ state a Voltage $V_p$ $(-V_q)$ is applied. A voltage $V_c$ or $-V_c$ is applied to operate the device is normal mode. One of the drawbacks of integrating ferroelectric capacitors directly with the split gates is the high supply voltage needed to perform the switching operation. This could be circumvented by adopting the complementary ferroelectric capacitor structure [11] where the voltage swing generated by the capacitive coupling effect of the capacitor pair is large enough to perform the switching action at low supply voltages.

## III. Constructing circuits using reconfigurable fabric

### A. Programming the Hexagonal Array

Our BDD reconfigurable fabric is a regular hexagonal packing of the BDD nodes. Each of the non-vertical edges of the hexagonal structure has a top gate as well as a split gate and each vertical edge is composed of a nanowire. Each BDD node can be configured to function in one of three states. Reconfigurability can be achieved by using the new device explained in the previous section. Every non-vertical edge in the hexagonal array is in its normal operating mode initially. By applying a positive bias voltage $V_p$ it can programmed into a short and by applying a negative voltage $V_q$ it can be programmed into an open edge. The programmed edge can be reset to normal mode by applying $V_c$ voltage. An edge once programmed remains in that state until another voltage is applied. This non-volatile nature of the split gate programming is the key to reconfiguration. We call the required programming voltage as $V_{pp}$ which is one of $V_p, V_q, V_c$.

A grid of nanowires is used to program an edge. In order to be able to program the hexagonal array, we need to be able to uniquely address an edge. At a crosspoint of the grid, the vertical and horizontal wires are connected through terminals to the split sidewall gates of an edge. Figure 8 shows how the programming takes place. The target crosspoint's vertical wire is held at $V_{pp}$ and the horizontal wire is connected to ground. The rest of the wires of the grid are maintained at $\frac{V_{pp}}{2}$. This enables us to uniquely configure an edge as the required programming voltage of $V_{pp}$ is present only across one edge. In addition, $\frac{V_{pp}}{2}$ is distinct from $V_c$ and thus, the device is reconfigurable. The already programmed edges do not interfere with the configuring of an edge. The technique is very similar to the antifuse programming. However, unlike the antifuse there are no new connections created due to programmed antifuses. Using this technique we would need $2n$ vertical and $n$ horizontal wires resulting in a total of $3n$ wires.

### B. Reconfigurable structures

In the normal mode, the control gate of the left segment is controlled by the variable x and that of the right segment is

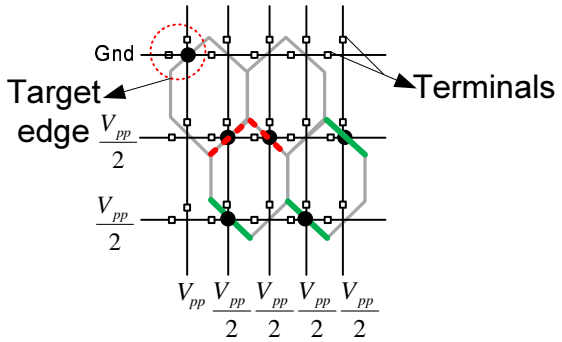


Fig. 8. Programming the hexagonal array

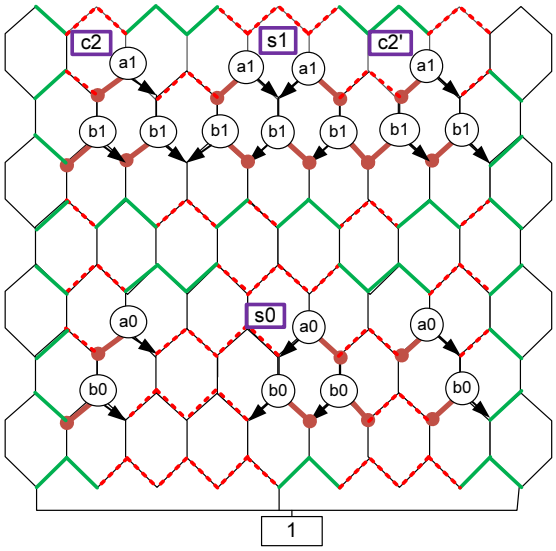


Fig. 9. 2-bit adder on a reconfigurable fabric. Programmable etching (dotted lines) or shorting (solid lines) when individual bias is applied to each split edge of a BDD node.

controlled by its complement x‘ or vice-versa. The individual segments of the BDD node can be configured to be completely open or short by biasing the split gates as illustrated earlier. This additional device feature enables ”programmable etching” or ”programmable shorting” as opposed to the custom fabrication of nanowires and lithographic etching. Consequently, one could configure a 2-bit adder as depicted in Figure 9 by modifying the split gate bias for every edge. The programmable feature also permits configurability between active high and active low output modes (not shown in picture). In the Hokkaido University work, all the zero terminals in the BDD were etched away and all the 1-terminals are connected to only a single 1-terminal. However, in our case using the programmable feature, we could have all the 1-terminals open and connect the zero terminals to Vdd. Such reconfigurability between active high or low modes can be very useful during testing the structures for leakage or defects.

An additional challenge in providing the reconfigurability concerns the lack of flexibility in connecting the inputs to the top control gates. In a custom design, it is possible to interchange the role of the left edge and right edge in different parts of the same BDD fabric row by swapping the x and x‘ control connections. This flexibility is lost in the reconfigurable fabric as the connections to the left and right edges are fixed at

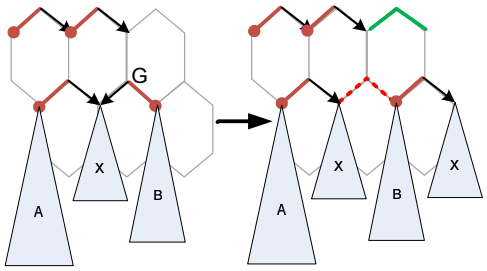


Fig. 11. Remapping a complemented pattern into the symmetric structure.

TABLE I
OVERHEAD IN TERMS OF EXTRA CELLS NEEDED FOR MAPPING ONTO DIFFERENT FABRICS

| Circuit | Fully custom | Overhead in Symmetric | Overhead Mirror | Overhead Sparse |
|---|---|---|---|---|
| C17 | 12 | 8 | 8 | 8 |
| Decoder(2to4) | 4 | 0 | 4 | 0 |
| n bit parity | n(n-1)/2 | 0 | (n(n-1)/2)-1 | (n+5)(n-2)/4 |
| 2-bit adder | 51 | 77 | 108 | 80 |

fabrication time (for every row). Supporting a multiplexor to make a choice between x and x’ to each sidewall gate control is not realistic. To circumvent this challenge, we explore a combination of architectural modifications and modified BDD mapping techniques.

### C. Symmetric Fabric

In the symmetric case (see Figure 13(a)), we have uniform rows in which a complete row has left edge connected to x and right edge connected to x’ or vice-versa. The result of such a symmetric mapping gives rise to BDDs of larger size due to the lack of complementary arc pattern. This does not compromise any BDD properties. The use of negated arcs is a well-known optimization in BDD structures for reducing the size of the BDD as it enables sharing of sub-BDDs. In case there are negated arcs for the same variable, we resolve it by flipping the node ($G$) and separating the sub trees as shown in the Figure 11. Note that the solution shown works for the case when the subtrees are non-overlapping and do not themselves have negated arcs. Separating the sub-trees gives rise to duplication of subtrees (in this case $X$) as can be seen from the figure.

If the subtrees have connections between them then we can always connect them without overlapping with other routes by using one edge as open and the other edge as closed (01/10 patterns). In case of overlapping trees as well as if the subtrees themselves have negated arcs, we use a bottom-up approach in order to resolve them. For example, consider the scenario in Figure 12. We first resolve the F1 node and then in the second step flip the F2 node. Using this procedure, we map some representative set of circuits. Table I(a) shows the overhead in terms of number of additional cells required over a non-reconfigurable design. Number of cells are counted within a boundary such as the one outlined in the Figure 10(a). Figure 10(a) shows a 2-bit adder when mapped onto a symmetric fabric.

### D. Other Fabrics

Another option is using mirror fabric in which each alternate BDD node in a row has the role of the left and right edge

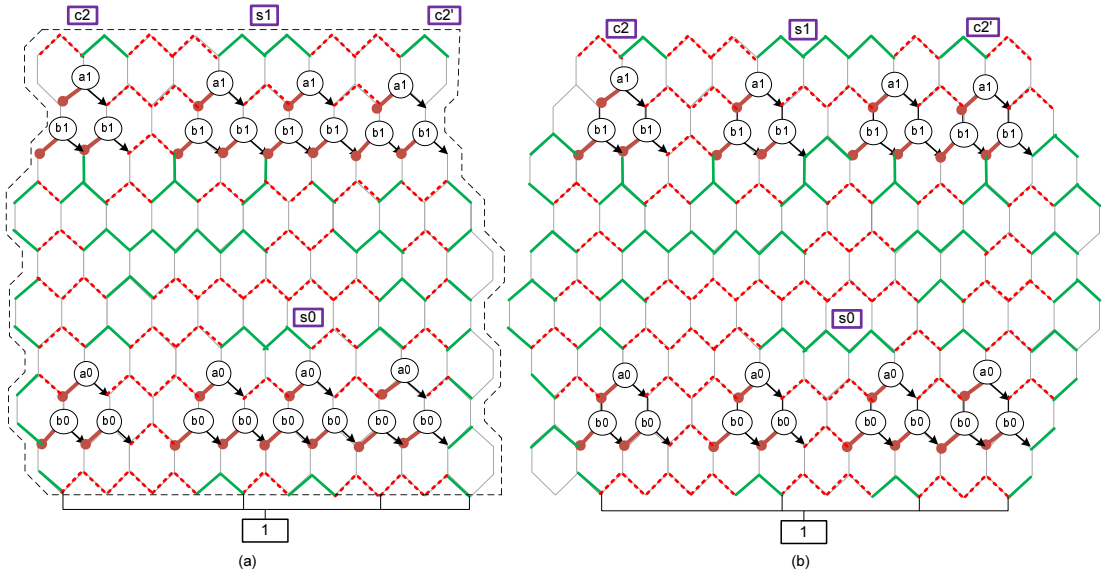


Fig. 10. 2-bit adder mapped onto (a) Symmetric fabric and (b) Symmetric fabric and using coarser granularity for programming

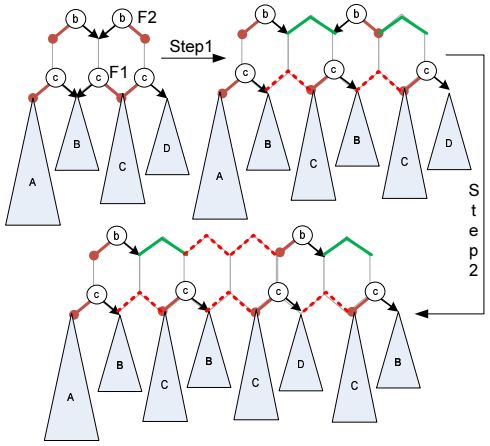


Fig. 12. Sub-BDDs overlap and contain negated arcs

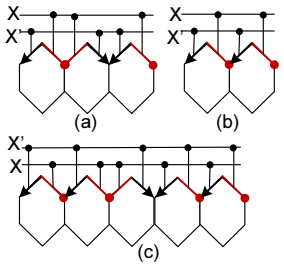


Fig. 13. (a) Mirror fabric (b) Symmetric fabric and (c) Sparse fabric

exchanged. Consequently, if the circuit is symmetric then only alternate nodes are utilized. We consider another fabric, which is intermediate between symmetric and mirror, in which the negated arcs appear after every two columns called sparse fabric, as negated arcs are not that frequent. We also map the ISCAS85 c17 circuit, a 2to4 decoder and a n bit xor circuit and the overhead is given in Table I(b). The parity circuit is a symmetric structure and hence mirror fabric gives rise to about 100% overhead. Symmetric layout is found to have the least overhead for mapping circuits. The different fabric patterns

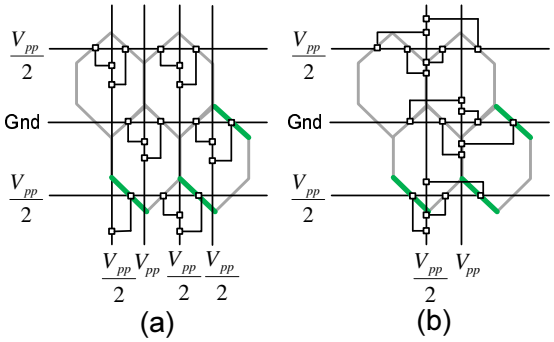


Fig. 14. The bias signal is shared between (a) two nodes and (b) four nodes

are summarized in Figure 13.

### E. Granularity of Control

To reduce the number of wires required to program the devices, we vary the number of devices sharing the same vertical wire/line as shown in figure 14. The new mappings with such a coarser grain programmable control requires adjacent devices to be in same operating state and causes additional area overhead. Figure 10(b) illustrates a representative tradeoff for realizing a 2-bit adder when common bias signal is used for both split gates corresponding to the two edges of a BDD node on a symmetric mapped fabric. The area of the mapped structure increases to 94 cells resulting in an overhead of 43 cells from the base custom design of 51 cells. If we increase the granularity of control from one node to 2 adjacent nodes as shown in Figure 14(b) i.e. four split gates then the overhead increses to 268 cells.

## IV. Related Work

This section is grouped into related work concerning devices and reconfigurable architectures.

**Devices:** There have been a number of reports on the fabrication of single electron device using quantum dots

coupled to source and drain contacts through tunnel barriers. Single electron phenomena at both low temperature as well as at room temperature have been reported and single electron devices fabricated in a variety of materials such as such as aluminium [12] heterostructures [13], [14] and silicon [15], [16], [17], [18], Recent progress in semiconductor nanotechnology has shown that quantum devices such as single/few electron transistors operating at room temperature are feasible [19], [20], thereby solving a "traditional problem" of quantum devices. Still, the quantum devices typically have poor driving capability and poor threshold control due to one/few electron involvement in the switching process. To solve the above problem, researchers from Hokkaido University have recently proposed a novel hexagonal binary decision diagram (BDD) circuit approach [7], [21], [22] (Figure 1(a)). The reconfigurable device structure is a key distinction of our work.

**Reconfigurable Architecture:** The last decade has seen large-scale concerted efforts to develop nano-scale technologies that will help sustain the Moore's law. Reconfigurability is a key feature in many of these nanoscale systems to ensure robust systems in the presence of high individual component defect rates. Further, these emerging technologies lend themselves to build regular programmable fabrics than complex customized designs. Examples of such reconfigurable architectures in emerging technologies include: nanowire-based architectures to tolerate defective and stochastic assembly of regular arrays in designing robust systems [23]; a nanofabric based on molecular electronics that discovers the characteristics of the fabric and then create circuits that avoid the defects and use the available resources [24] and a reconfigurable architecture using hybrid CMOS and nanowire technology proposed in [25]. Our work is complementary to these efforts in exploring programmability in BDD style logic as well as introducing programmability using a new quantum device structure.

## V. Conclusion

One of the promising few electron devices that operate in quantum domain and exhibit low transconductance, are the quantum nanowire based wrap gate device. Binary decision diagram (BDD) based logic using these ultra low power devices have been demonstrated in earlier work. BDD structures present a very attractive way for designing logic. The logic built out of nanowire devices, however have a fixed structure and are not reconfigurable. Reconfigurability is vital for nanoscale devices due to the predicted high defect rate and device variability. Lack of reconfigurability is a serious concern and we address this issue. We propose a novel device architecture that supports non-volatile programmability using ferroelectric capacitors and split gates. We propose system architectural modifications to incorporate such a device in logic design. Mapping challenges have been identified and solutions have been provided for target circuits.

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