Nanoelectronics • Architectures

MIND

MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY

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R E S E A R C H   I N I T I A T I V E

Final Executive Summary

The Midwest Institute for Nanoelectronics Discovery (MIND) was announced on March 26, 2008, at Notre Dame with backing and support of the Semiconductor Research Corporation, the National Institute of Standards and Technology (NIST), the State of Indiana, the City of South Bend, and the University of Notre Dame. The founding universities were Notre Dame, Penn State, Purdue, Illinois, Michigan, and UT Dallas. The total research investment was approximately $20M. As important as this funding was in launching MIND, the center benefited from the collective support of IBM, the University of Notre Dame, bipartisan support in Indianapolis, and leadership in the City of South Bend, which used MIND as an example of a productive university/industry collaboration with the aim of job creation. The economic development leaders in South Bend and Elkhart were consistent supporters of MIND through the five year period of the center.

In 2008 MIND became the fourth center in the Nanoelectronics Research Initiative (NRI), adding tunnel field-effect transistors (TFETs), nanomagnet logic (NML) technology, and explorations in plasmonics, graphene spin FETs, and thermal devices to the widening suite of devices under exploration in the NRI. To better understand and compare the NRI emerging device technologies, MIND proposed and initiated a benchmarking activity, which has been refined in each year to help guide and gauge the relative merits of the devices under development across the NRI. This effort was led by Kerry Bernstein of IBM Research, who was able to win support for the benchmarking effort across all of the centers. MIND also set as a task the exploration of new architectures to utilize NRI device technologies and again, led by Kerry Bernstein, ran architecture workshops in the early years to stimulate researchers to think broadly about the ways to use non-charge-based technologies. MIND held four architectures and benchmarking workshops on the day before the MIND annual review each year to stimulate consideration of new ways to utilize NRI technologies for computation.

MIND benefited significantly from collaborations with NIST, Argonne National Laboratory, and the National High Magnetic Field Laboratory. A MIND postdoc, Qin Zhang, from Notre Dame worked at NIST in Gaithersburg for three years on graphene and III-V TFET metrology. This was a highly productive collaboration with NIST, resulting in 10 journal publications and 15 conference papers. The internal photoemission (IPE) measurement system of Nhan Nguyen, NIST, was utilized extensively in TFET transistor development to determine the flat band voltage and band alignments in graphene and III-V TFETs. NIST has also hosted graduate students from Purdue, Penn State, and Notre Dame for extended stays to utilize the IPE measurement capability and for pulsed current-voltage measurements. MIND students made trips to Argonne to utilize their x-ray photoemission electron microscope for imaging nanomagnets, and to the National High Magnetic Field Laboratory for magnetotransport measurements

Since March of 2008, MIND through October of 2012 MIND researchers generated 496 publications, including journal and conference papers. In 55 months, this is an average of approximately 9 publications per month over the duration of the center or about two publications per week. This is for a research team that averaged about 65 researchers including 21 faculty, plus post docs and graduate students. IBM provided an assignee to the center over most of the duration of the center. MIND researchers filed for four patents relating to nanomagnet logic, TFETs, and teraherz modulators. One patent on nanomagnet logic and one on tunnel FETs issued with two pending.

In 2011, the NRI centers were asked to recompete and focus on one or two devices. In consultation with the industry mentors, MIND focused resources on TFET and NML technologies and dropped work on plasmonics, thermal logic, and graphene spin-based devices. The technologies that were dropped were not been successful in identifying a clear and compelling basis for a logic technology. The primary objective in MIND phase 1.5 has been to systematically explore TFET and NML technologies and produce experimental data to enable a quantitative assessment of the performance of both technologies for scaling beyond the limits of CMOS. For the TFET, the goal was set to demonstrate device technology to meet the theoretical predictions for low subthreshold swing, high on-current, and low off-current, at sub-half-volt supply voltages. For NML, the goal was to demonstrate logic circuits that enable evaluation of the low-power performance potential of the technology. Since NML is well suited to systolic architectures, the focus of the technology development has been toward clocked systems.

Most significant research achievements of the center over its history

III-V tunnel FETs. Prior to MIND, there were no demonstrations of tunnel FETs in III-V materials, and the results in group IV materials were not clear (the junctions were just not abrupt enough to show negative differential resistance in the forward bias direction). The first demonstration of the III-V TFET was achieved by Penn State in 2009 using a *p-i-n* InGaAs homojunction utilizing a sidewall gate, with gate field oriented obliquely to the current direction (Mookerjea et al. IEDM 2009). This was followed by a study of the temperature dependence (Mookerjea et al. *EDL* 31 2010) and steady improvements in on-current with the introduction of heterojunctions (Mohata, IEDM 2011, *Appl. Phys. Exp.* 4 2011, Bijesh VLSI Symp. 2012). Purdue proposed a geometry with gate field oriented in-line with the current direction (Klimeck patent filed 2010, Agarwal et al. *EDL* 31 2010), and Notre Dame proposed III-V embodiments (Seabaugh et al. patent filed 2011), which were then demonstrated (Li et al. *EDL* 33 2012, Zhou et al. *EDL* 33 2012, etc.). Record current density in III-V TFETs now stands at 180 μA/μm at 0.5 V (Zhou et al. IEDM 2012), but similar currents are also obtained in the sidewall gate TFET by Penn State. The first *p*-channel TFETs have just recently been demonstrated at Penn State. Scaling has also been pushed in MIND using the nanoassembly process of Penn State (Morrow et al. *Science* 323 2009) and device fabrication approach from the same laboratory (Ho et al. *Nano Lett.* 8, 2008). In collaboration with Bob Wallace, understanding of best practices for gate surface preparation, passivation, and leakage reduction have been steadily advancing. Analytic modeling in MIND now shows that the drive to higher on-current must be traded off against off-current and that there is an optimum bandgap for a given supply voltage, on-current, and off-current (Zhang et al. DRC 2012 late news).

Graphene TFETs and beyond. Several of the most highly cited papers in MIND have been written under this task. *The* most highly cited paper (Fang et al. *PRB* 78 2008) models transport in graphene nanoribbons, comparing the effects of phonon, impurity, and line-edge roughness scattering with application to improving mobility. A paper entitled "Graphene nanoribbon tunnel transistors" is the second most highly cited paper in MIND (Zhang et al. *EDL* 29 2008). This paper shows that graphene nanoribbon TFETs can simultaneously achieve both high speed and low power dissipation. The graphene TFET task also has many experimental highlights, including demonstration of a wafer scale fabrication process for graphene (Tahy et al. DRC 2011), process techniques for forming 10 nm nanoribbons (Hwang et al. *JVST B* 30 2012), demonstration of the opening of a bandgap (Hwang et al. *Appl. Phys. Lett.* 100 2012), and record on-current of 10 mA/μm in nanoribbon FETs (Hwang, ISCS 2012). This year, *p-n* junctions have been demonstrated using side gates and ion doping in nanoribbon TFETs with the observation of negative differential resistance at room temperature. It has also been shown theoretically that the symmetric bandstructure of graphene enables a new kind of switch based on tunneling between graphene bilayers (Feenstra et al. *J. Appl. Phys.* 111 2012). A transistor based on this junction phenomena has been invented which should exhibit both negative resistance and negative transconductance (Zhao et al. DRC 2012). Two-dimensional (2D) crystal materials have also been explored. These materials allow development of TFETs without the need to form nanoribbons to open a bandgap; 2D crystal FETs have also been demonstrated in WS_2 (Hwang et al. *Appl. Phys. Lett.* 101 2012) and $MoTe_2$.

Atomistic device modeling. Modeling insights on TFET leakage paths and experimental realities such as growth capabilities and graphene line-edge roughness drove atomistic device modeling within OMEN/NEMO5 to incorporate new capabilities. These new capabilities were built under funding leveraged from NSF and explored under MIND funding. This led to a new tool set that can analyze complex geometries such as layered lateral devices that suppress leakage and optimize current on/off ratios. The modeling capabilities go far beyond standard commercial TCAD and are foundationally implemented in a new community code NEMO5. This new code is now in use at Intel, GLOBALFOUNDRIES, IBM, Samsung, and Lockheed Martin.

Nanomagnet logic. Following demonstrations of the fundamental building blocks for NML circuits, Notre Dame (ND) has concentrated on the dynamic properties of nanomagnets, ways to read, write, and clock NML structures, and suitable architectures for this technology. Clock designs were devised that enabled the local control of NML ensembles, and still led to "wins" over transistor-based hardware with respect to energy. These designs were then experimentally demonstrated, and used to locally control NML devices (Alam et al. TNANO 2010), Boolean logic gates, and interconnect (Alam

et al. TNANO 2012). As the need for clocking impacts dataflow, *i.e.,* it creates inherent pipelines, application-level architectures were identified such that information processing tasks, *e.g.,* pattern matching for "big data," could be accomplished efficiently (Niemier et al, CNNA 2012). State-of-the-art transistor-based equivalents were also designed and benchmarked. Specific outcomes from this effort include (i) revised clock designs, and (ii) proposals for enhanced permeability dielectrics to further minimize clock energy. Notably, this later work seeded experimental work that suggests that clock energy can be reduced by as much as 30x (Li et al. *IEEE Trans. Magnetics* 48, 2012).

Any new technology based on alternative state variables should be able to interface with charge-based devices in an efficient manner. Toward this end, four candidate output structures were considered to move information from the magnetic domain back to the electrical domain (Liu et al., TNANO 2011). The same clock structures can also be used to properly set the state of an output device. The Notre Dame design targets were fabricated at IBM via a DARPA-funded collaboration. Electrical input structures were also developed and successfully tested at ND.

Finally, ND also: (i) employed micromagnetic simulations to design circuits that enable more complex and efficient computer architectures *e.g.,* reduced area gates (Niemier et al., US Patent No. 8,058,906), fanout, and wire crossings, (ii) considered how clocking could impact nonvolatility (Dingler et al. DAC 2012), (iii) studied how fabrication variations impact logic correctness and clock energy, and (iv) fabricated and successfully tested full adder structures (Varga et al. Intermag/MMM 2013). The Varga accomplishment appears to be the first demonstration of concatenated gates using spin-based devices.

Future directions

Steeper transistors. Steeper transistor slopes and lower voltages should be possible in 2D materials like graphene and dichalcogenide crystals because of self-passivated surfaces and excellent electrostatics. The symmetric band structure enables complementary operation and atomically thin dimensions beyond the limits of scaling of any FET. The III-Nitrides allow the incorporation of piezoelectricity and spontaneous polarization into the design of steep transistors. Complex oxide heterostructures supporting an atomically abrupt and super-high-density 2D electron gas offering a further intriguing platform for low-voltage steep transistors.

Atomistic device modeling. The emergence of new materials to be explored in tunneling transistors such as III-Nitrides, 2D materials, and complex oxides is driving new modeling requirements. The material properties are barely known and need to be explored via experiment and *ab initio* materials models. Subsequently, this foundational data must be mapped into atomistic tight-binding that can scale to realistic device sizes via NEMO5. Ongoing and future NEMO5 endeavors embrace the foundational *ab initio* mapping to tight binding. Furthermore, the relative importance of scattering mechanisms must be examined as well as the interactions between collective phenomena such as piezoelectric responses to local charge densities.

Nanomagnet logic. The research directions for NML should be expanded to include devices with perpendicular magnetic anisotropy (PMA) that are clocked with electric fields. NML devices with PMA (pNML) are especially advantageous when considering system architectures: (1) Provided inputs do not change, the potential for data races associated with different signal arrival times at an in-plane NML gate can be eliminated in pNML circuits. (2) pNML devices always couple antiferromagnetically to neighboring devices, and can be resized such that neighboring devices have different footprints. This reduces the complexity of local signal routing. pNML wire crossings have been realized. (3) With pNML, focused ion beam (FIB) irradiation can define dataflow directionality *without* the multiphase clock schemes that are required for in-plane NML. This also enables fine-grained pipelining and higher throughputs. (4) pNML opens the door to multiple layers of metallic devices that couple in a third dimension. This not only reduces circuit area but can also increase device-to-device coupling (which will reduce error rates), and provides the ability to create circuits with high fan-in. Focus on the design of pNML-based Boolean and non-Boolean logic appears promising. Particular attention should be given to efficient interconnect where propagating domain walls seem promising. Stochastic computing architectures could enable useful information processing hardware using these devices.

Executive Summary for the Last Six Months

The on-currents in *n*-TFETs have been improved and record performance is now demonstrated in both the Penn State *p-i-n* sidewall gate geometry and the Notre Dame *p-n* in-line gate geometry. With V_{DS} = 0.5 V, on-currents of 135 and 180 µA/µm, respectively, have been demonstrated. TFETs with p-channels have been designed and grown for fabrication by both Penn State and Notre Dame. Penn State has initial demonstrations showing transistor action, the first III-V *p*TFETs. Both Notre Dame and Penn State now have pTFETs in process. Comparisons of TCAD and atomistic NEMO5 has proceeded to validate the design approach for both *n* and *p* channel TFETs and graphene TFETs. New physics has been added to NEMO5 to allow consideration of bandgap narrowing, alloy and interface disorder, and discrete impurity effects. Processes for sub-50-nm III-V nanopillars were developed and annealing and etch protocols were found which reduce the surface leakage by three orders of magnitude following RIE etch. Processes for forming and releasing fins for directed assembly were demonstrated to enable development of nanoscale TFETs. Penn State and Notre Dame continue to work closely with UT Dallas to build core understanding of the oxide/semiconductor interface and tangential subthreshold swings as low as 93 mV/decade have been observed. In graphene, methods to form and dope graphene nanoribbons have lead to demonstration of NDR in a graphene nanoribbon. Both MoS_2 and WS_2 offer 2D crystals which do not require the formation of a nanoribbon to enable the TFET. FETs in both materials were demonstrated. A new type of gated field-effect transistor in 2D materials was invented utilizing tunneling across 2D crystal planes separated by an oxide.

This year the work in NML expanded from consideration of in-plane magnetization based on patterned magnetics, to structures in which the magnetism is perpendicular to the plane, now referred to as perpendicular magnetic logic (PML). PML is of interest because it can be clocked with homogeneous and *global* magnetic fields, which simplifies the drive circuitry, and opens up new approaches for signal routing and system architecture. A crucial element for NML is the clock, which provides the magnetic field needed to switch the individual nanomagnets. Reducing clocking energy for NML is an important goal of this research and experiments this year with enhanced permeability dielectric (EPD) materials to clad the clock wires have shown that the field confinement can reduce the current needed to clock a nanomagnet. For stand-alone magnets, the EPD films have helped to lower the nulling clock field from 160 mT to 65 mT (~60% reduction). The same trend is seen in the sample of coupled magnets, where the nulling clock field decreases to 40 mT from 160 mT, a 75% reduction. EPD films can be used not only to reduce the switching energy of clock wires, but also have utility for increasing magnetic coupling between adjacent nanomagnets.

MIND researchers responded to the industry requests to unify the benchmarking assumptions for TFETs and NML. Data was provided to the member companies. The results of this reassessment were presented at the Notre Dame Architectures and Device Benchmarking Workshop held in August 2012.

THEME 1: Tunnel field-effect transistors
Theme Leaders: G. Klimeck, P. Fay, S. Datta, T. Mayer, R. Wallace, D. Jena
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Theme 1 Executive Summary

Purdue (Klimeck): The Klimeck research group enhanced the NEMO5 code for TFET exploration at the ultimate scaling limit. This year bandgap narrowing, alloy and interface disorder, and discrete impurity effects were added. The past several months focused on comparison of NEMO5 simulations against standard TCAD tools. The comparisons against standard TCAD tools show that NEMO5 can expose some of the more fundamental limits of the off currents and the subthreshold swing that are not captured by standard TCAD models. NEMO5 was used to explore designs in GaSb/InAs staggered gap materials. Furthermore, the design options through ternary alloys in GaAsSb have been explored. In particular, issues of critical undercut lengths to suppress off- current were explored and shared with the experimental efforts in Seabaugh's group. In another experiment/theory collaboration, quantum transport modeling tools were used to explore the GNR TFET and compare against the original analytical model designs. Both modeling and experiment show negative differential resistance (NDR) in the reverse bias direction, confirming band-to-band tunneling.

Notre Dame (Fay): In-line geometry n-channel TFETs with record on-current density of 180 µA/µm at V_{DS} = 0.5 V were demonstrated in the broken-gap InAs/GaSb heterostructure. I_{ON}/I_{OFF} ratios of 6 x 10^3 were obtained, with a minimum subthreshold swing of 150 mV/decade. First exploration of the lattice-matched ZnTe/InAs heterojunction grown by MBE was completed. Transmission electron micrographs show a defect free interface. Capacitance voltage characteristics show extracted interface state densities of 1-3.5 x 10^{11}/cm^2eV. In-line p-channel TFETs were designed, selective etch stops were calibrated and the first structures are in process.

Penn State (Datta): Experimental study of the effect of heterojunction band alignment on the n-channel GaAs$_{0.35}$Sb$_{0.65}$/In$_{0.7}$Ga$_{0.3}$As TFET showed that record I_{ON} (135 µA/µm at V_{DS} = 0.5 V) could be achieved by engineering to form the lowest source-channel tunneling barrier height. Fabrication and testing of the first p-channel In$_{0.7}$Ga$_{0.3}$As/GaAs$_{0.35}$Sb$_{0.65}$ TFETs was completed showing transistor action. A multicore TFET- CMOS architecture was explored and it was found that at 21% speed improvement could be obtained relative to the CMOS-only core; this resulted in a best student paper award at the 2012 CODES Conference.

Penn State (Mayer): Processes to reduce the edge leakage in sub-50-nm diameter reactive-ion etched InGaAs nanowires were demonstrated to reduce leakage by over three orders of magnitude. An efficient process for creating etched heterojunction TFET fins was developed which allows the fins to be released into solution and then deterministically reassembled on a patterned substrate for subsequent processing into TFETs arrays.

UT-Dallas (Wallace): The stability of the InAs(100)/crystalline oxide interface to Al$_2$O$_3$ atomic layer deposition was investigated. After the first metal precursor pulse, the LEED pattern showed an unreconstructed surface, suggesting that the interface is not stable upon TMA exposure. In a collaboration with Datta (Penn State), TFET gate stacks on GaAsSb were studied *in situ*, and As-As bonding was detected at the HfO$_2$/Al$_2$O$_3$/GaAsSb interface upon exposure to the ALD process. Such bonding is typically associated with a defect level that results in pinning.

Notre Dame (Jena): Building on the GNR fabrication process, room-temperature NDR in gated GNR p-n junctions was demonstrated. Li and ClO$_4$ ions in polyethylene oxide were drifted into place along the GNR using side gates, to form the p-n junction. The NDR has been modeled using both semi-analytical and NEGF-based simulations and the results are consistent with the experiment. Further consideration of graphene-insulator-graphene junctions has lead to the invention of a transistor, called the SymFET, that exploits the bandstucture symmetry of graphene for a transistor which exhibits both NDR and negative transconductance. Experiments with 2D crystal semiconductors such as MoS$_2$ show another route for TFETs to achieve without the need for a nanoribbon to open induce a bandgap.

Modeling and analysis of tunnel transistors with NEMO/OMEN – G. Klimeck (Purdue)

The Klimeck group has been working with the Notre Dame group to understand the physics of graphene nanoribbon tunneling field-effect transistors (GNRTFET). Our goal is to fabricate a novel GNRTFET that can operate at a subthreshold swing of less than 60 mV/dec. The Notre Dame group has fabricated a GNRTFET based on an electrical doping through side gates. The device dimensions are still too large for a TFET to operate in a sub-60 mV/dec regime. However, we are trying to understand the physics of the device through atomistic simulations and to propose a better structure. The measured negative differential resistance (NDR) is captured by the atomistic simulation, and a very small ballistic efficiency (0.2) and long mean free path (500 nm) is observed. This effect can be attributed to the reduced electron-phonon scattering due to ions at the GNR surface. More in-depth analysis is needed to explain this phenomenon. As a separate project, GNRTFETs in extremely scaled dimensions (width < 5 nm) has been studied where the operational characteristics of GNRTFETs can be optimized. This study is carried out through the Klimeck group's atomistic simulation (Tight-Binding) and the Notre Dame group's analytical modeling (WKB). The Klimeck group's simulator was calibrated with ab-initio calculation. The Notre Dame group has been calibrating their analytical modeling with the Klimeck group's atomistic simulator. After matching the imaginary band structure and the conduction band diagram at the OFF state of the p-i-n GNRTFET, the transmission probability from the source to the drain was calculated. For a smaller bandgap (0.25 eV) device, the analytical transmission is similar to the transmission calculated by the atomistic simulator. However, for a larger bandgap (0.65 eV) device, the difference between these two models becomes significantly large.
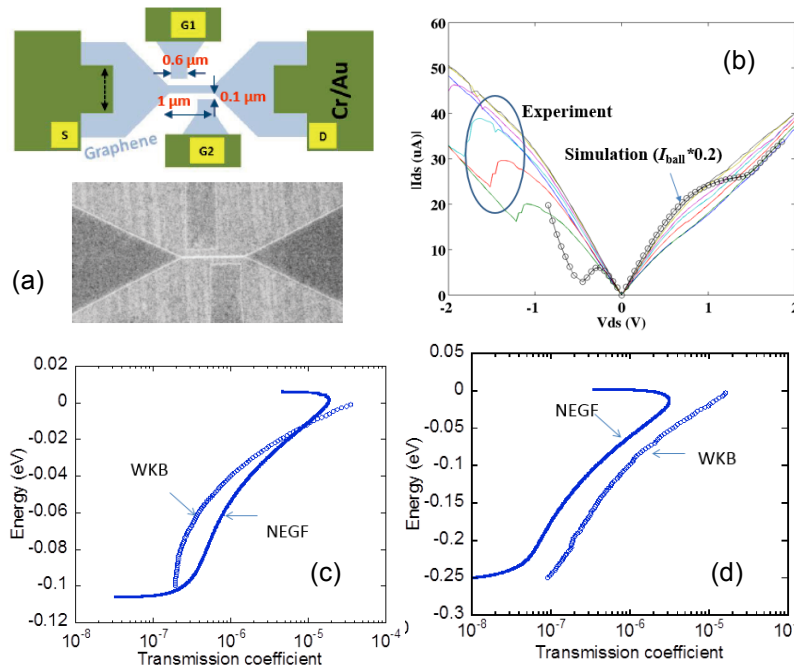

Figure: (a) a schematic diagram and a TEM image of a fabricated GNRTFET (b) the experimental Id-Vd characteristic of GNRTFET compared with atomistic simulation results, the transmission probability from the source to the drain of p-i-n GNRTFETs for (c) a smaller bandgap device (Eg=0.25 eV, width=5.15 nm) and (d) a larger bandgap device (Eg=0.65 eV, width=2 nm)

Our work on III-V TFETs continues to focus on staggered band-gap materials, in particular GaSb/InAs. We simulated performances of AlGaSb/InAs TFETs. As the first step, a lattice matched structure is assumed and local strain variations are ignored. Performance deviations in terms of atom type variations are evaluated. Then we computed bandgap variation in random alloy GaInAs structures with more realistic strain profiles calculated by VFF. It is found that strain variation will have great impacts on bandgap, and anharmonic strain model is important to capture the bowing factor for continuous change of bandgap with alloy composition. Further simulations of realistic alloy transport with strain are limited by computational burdens and strain dependent tight-binding parameters. Given experimental data on measured bandgap, we are using virtual crystal approximation to match the bandgap changes, even with bandgap narrowing effects. This allows performance evaluations as a first order approximation.

Moving forward our goal is to simulate quantum transport in atomistic alloy III-V structures and the GNRTFETs in close collaboration with the experimental groups at Notre Dame and Penn State. With the atomistic random alloy, we have encountered computational intensity issues we did not anticipate. We are in the process of optimizing the speed of the code to enable true disordered alloy transistor simulations.

Heterojunction *p-n* TFETs – P. Fay, T. Kosel, A. Seabaugh, G. Xing, M. Wistey (ND)

Tunnel FETs based on the in-line geometry have been investigated. Following the geometric and heterostructure design insights obtained previously, devices with record on-current densities of 180 µA/µm at V_{DS} = 0.5 V were obtained in the InAs/GaSb material system for a broken-gap alignment, consistent with predictions from TCAD modeling. Figure 1 shows the common-source and transfer characteristics of this device. An I_{ON}/I_{OFF} ratio of 6×10^3 was obtained for $V_{DS} = V_{GS} = 0.5$ V. The dependence of subthreshold swing on processing conditions was also evaluated, with the lowest swing obtained for
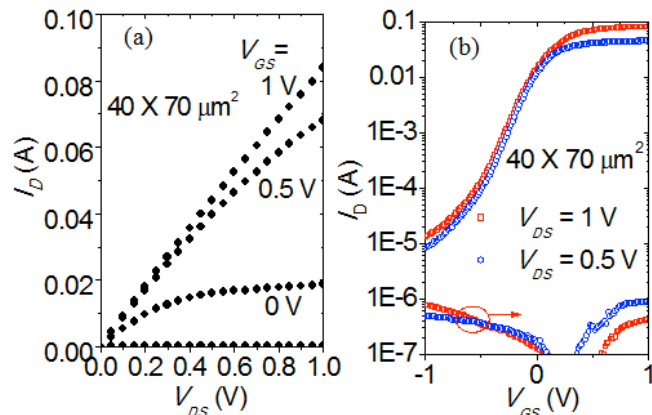

Figure 1. Common-source and transfer characteristics of InAs/GaSb broken-gap in-line TFET. A record drain current density of 180 µA/µm at V_{DS}=0.5 V has been obtained.

passivated devices after annealing in forming gas (Figure 2). A minimum SS of 150 mV/decade was obtained, limited by interface states. TCAD simulations of geometries with similar electrostatics suggest slopes well below 60 mV/decade should be expected, indicating the role of interface states. To address the high D_{it} obtained at the InAs/high-k interface, MBE-grown ZnTe on InAs was investigated as a possible gate dielectric. As shown in Figure 3, cross-sectional TEM reveals an epitaxial interface with no evidence of dislocations. Low-temperature C-V suggests a D_{it} for the InAs/ZnTe interface of $1 - 3.5 \times 10^{11}$ /cm^{2}eV. TCAD simulations indicate that this level of interface states is promising for enabling sub-60 mV/decade swings to be achieved. In addition to these device demonstrations, work is ongoing to demonstrate in-line p-TFETs based on GaSb/InAs broken-gap junctions, with the first heterostructures currently in process.
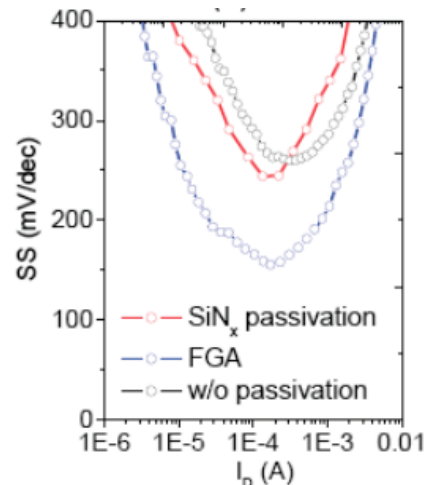

Figure 2. Subthreshold swing dependence on processing, including passivation and forming gas anneal. A minimum SS of 150 mV/decade is obtained for passivated devices after anneal.

Publications and presentations since July 1, 2012:

- A. Seabaugh, "Tunnel field-effect transistor perspective," invited, International Symposium on Compound Semiconductors, August 2012, Santa Barbara, CA.
- Q. Liu, L. Dong, Y. Liu, R. Gordon, P. D. Ye, P. Fay, and A. Seabaugh, "Frequency response of LaAlO$_3$/SrTiO$_3$ all-oxide field-effect transistors," *Solid-State Electronics,* 76, 2012, 1-4.
- Q. Zhang, R. Li, T. Kosel, H. Xing, A. Seabaugh, K. Xu, O. A. Kirillov, C. A. Richter, D. J. Gundlach, and N. V. Nguyen, "Band offsets of Al$_2$O$_3$ on InAs/AlGaSb heterojunction measured by internal photoemission," accepted poster, IEEE Semiconductor Interface Specialists Conference, Dec. 2012, San Diego, CA.
- M. I. Shams, Y. Xie, Y. Lu, and P. Fay, "An accurate interband tunneling model for InAs/GaSb heterostructure devices," International Symposium on Compound Semiconductors, Santa Barbara, CA, Aug. 2012, Santa Barbara, CA.
- Q. Zhang, R. Li, R. Yan, T. Kosel, H. G. Xing, A. Seabaugh, K. Xu, O. A. Kirillov, D. J. Gundlach, C. A. Richter, and N. V. Nguyen, "A unique photoemission method to measure semiconductor heterojunction band offsets," submitted, *Appl. Phys. Lett.,* 2012.
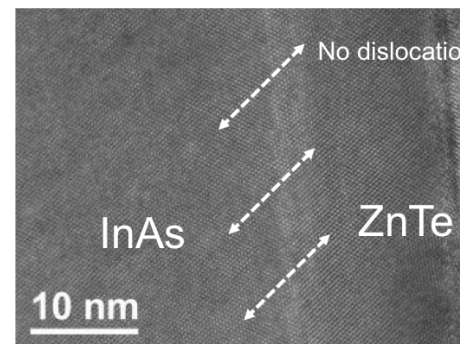

Figure 3. MBE-grown ZeTe on InAs. Low-temperature C-V reveals a D_{it} of 1-

Heterojunction *p-i-n* tunnel transistor logic & arch. – S. Datta, V. Narayanan, T. Mayer (PSU)

In the first half of 2012, we focused on improving the electrostatics and I_{ON}/I_{OFF} ratio in heterojunction *n*-channel TFETs. We succeeded in experimentally demonstrating enhancement in drive current I_{ON} and reduction in drain-induced barrier thinning (DIBT) in arsenide-antimonide staggered-gap heterojunction (hetj) tunnel field-effect transistors (TFETs) by engineering the effective tunneling barrier height Eb_{eff} from 0.58 to 0.25 eV. Moderate-stagger $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ (Eb_{ef} = 0.31 eV) and high-stagger $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ (Eb_{eff} = 0.25 eV) hetj TFETs are fabricated, and their electrical results are compared with the $In_{0.7}Ga_{0.3}As$ homojunction (homj) TFET (Eb_{eff} = 0.58 eV) (see Fig. 1. Due to the 57% reduction in Eb_{eff}, the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ hetj TFET achieves 253% enhancement in I_{ON} over the $In_{0.7}Ga_{0.3}As$ homj TFET at V_{DS} = 0.5 V and $V_{GS} - V_{OFF}$ = 1.5 V. With electrical oxide thickness (*Toxe*) scaling from 2.3 to 2 nm, the enhancement further increases to 350%, resulting in a record high I_{ON} of 135 µA/µm

Figure 1. Measured output characteristics of the fabricated devices. I_{ON} increases by 253% due to a decrease in Eb_{eff} from 0.58 to 0.25 eV [Ref 1]

and 65% reduction in DIBT at V_{DS} = 0.5 V. In the second half of the year, we shifted focus (based on NRI TAB feedback) to *p*-channel TFET epi layer design and device fabrication. Detailed structural properties and band offset determination of *p*-channel staggered gap $In_{0.7}Ga_{0.3}As$ source/ $GaAs_{0.35}Sb_{0.65}$ channel heterostructure tunnel field-effect transistor (TFET) grown by molecular beam epitaxy (MBE) were investigated. High resolution x-ray diffraction revealed that the active layers are strained with respect to the "virtual substrate." Dynamic secondary ion mass spectrometry confirmed an abrupt junction profile at the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface and minimal level of intermixing between As and Sb atoms. The valence band offset of 0.37 ±0.05 eV was extracted from x-ray photoelectron spectroscopy. A staggered band line-up was confirmed at the heterointerface with an effective tunneling barrier height of 0.13 eV. Functional *p*-channel TFETs were fabricated and characterized. The high *Dit* near the valence band resulted in poor electrostatics and low I_{ON} in the first generation of *p*HTFETs. Experiments are in progress and devices are being fabricated to address the high *Dit* issue and to improve the on-current performance of *p*HTFETs.

On the TFET architecture front, we evaluated a 32-core TFET-CMOS heterogeneous multicore processor. In order to effectively utilize this heterogeneous processor, we propose a novel automated runtime scheme. Our scheme is designed to automatically improve the performance of applications running on heterogeneous CMOS-TFET multicores operating under a fixed power budget, without requiring any effort from the application programmer or the user. Our scheme combines heterogeneous thread-to-core mapping, dynamic work partitioning, and dynamic power partitioning to identify energy efficient operating points. With simulations we show that our runtime scheme can enable a CMOS-TFET multicore to serve a diversity of workloads with high energy efficiency and achieve 21% average speed up over the best performing equivalent homogeneous multicore. This work was nominated for the best student paper award in the 2012 CODES conference.
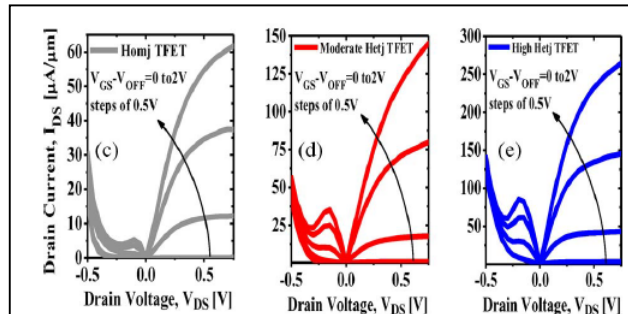
Publications and presentations since July 1, 2012:

- D. K. Mohata, R. Bijesh, T. Mayer, J. Fastenau, D. Lubyshev, A. K. Liu, and S. Datta, "Barrier engineered arsenide-antimonide hetero-junction tunnel FETs with enhanced drive current," *IEEE Electron Dev. Lett.,* vol. 33, no. 11, pp. 1568-1570, 2012.
- Y. Zhu, N. Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M. K. Hudait, "Structural properties and band offset determination of p-channel mixed As/Sb type-II staggered gap tunnel field-effect transistor structure," *Appl. Phys. Lett.* 101, 112106, 2012.
- R. Mukundrajan, M. Cotter, V. Saripalli, M. J. Irwin, S. Datta, and V. Narayanan, "Ultra low power circuit design using tunnel FETs," IEEE Computer Society Annual Symposium on VLSI, Aug. 2012, Amherst, MA.
- E. Kultursay, K. Swaminathan , V. Saripalli, S. Datta , V. Narayanan, and M. Kandemir, "Performance enhancement under power constraints using heterogeneous CMOS-TFET multicores," accepted, IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis, Oct. 2012, Tampere, Finland.

Nanofabrication platform for 1D nanowire tunnel transistors – T. Mayer, S. Datta (PSU)

This task aimed to study electrostatic and 1D scaling effects in the parallel tunneling structure by fabricating and characterizing arrays of sub-50 nm diameter InGaAs nanowire TFETs devices. To achieve this goal, we pursued two parallel objectives: (1) studying the impact of post-RIE surface treatments on ungated vertical TFET leakage, and (2) fabricate lateral p^+-i-n^+ InGaAs nanowire junction arrays using a process that can be scaled to sub-50 nm diameters.

To investigate the origin of the high reverse leakage current in high-aspect-ratio dry etched structures, vertical InGaAs pillar p^+-i-n^+ TFET structures with different orientations, geometries, and perimeter-to-area (P/A) ratios were fabricated by defining the pillars using either a wet etch or a $Cl_2/Ar/H_2$ RIE (Figure 1). To determine the effectiveness of post-etch thermal treatment in reducing RIE-induced leakage, the fabricated devices were subjected to a 20-min. thermal anneal at 350°C in both N_2 and N_2/H_2 following electrical measurement. The current density vs. voltage (J-V) properties of wet and dry etched <001> oriented fins with different P/A

Figure 1. (a) FESEM images of RIE (left) and wet etched (right) vertical InGaAs pillar p^+-i-n^+ TFET devices. (b) J-V characteristics of wet and dry etched InGaAs <01$\underline{1}$> fins with different P/A ratios and thermal treatment conditions.

ratios and annealing conditions are plotted in Figure 1. The reverse leakage measured at -1 V prior to annealing increases with the P/A ratio, suggesting that the current is dominated by surface leakage. The leakage current dropped by almost three orders of magnitude following thermal annealing in both N_2 and N_2/H_2 (not shown). However, in the low reverse bias region, the leakage was still higher and the voltage dependence is different for RIE than for pure wet etch. Ongoing temperature dependent J-V and device modelling efforts will reveal the mechanisms responsible for the increased leakage before and after thermal treatment.

The previously developed hybrid integration process has shown great promise in fabricating dense arrays of small diameter lateral nanowire TFETs. As illustrated in Figure 2, vertical p^+-i-n^+ InGaAs fins (step 1) are first dry etched using the same $Cl_2/Ar/H_2$ chemistry as the large-area pillars. The fins are then thinned to a width of 50 nm using a citric acid-based wet etch (step 1), and they are released from the InP substrate by selective wet etching (step 2). The solution-suspended fins are then deterministically assembled into lithographically defined features on a Si substrate (step 3). This assembly and integration process enables lateral device configurations where the heavily doped junctions are parallel to the substrate. With tiles registered to predefined lithographic markers, a resist pattern consisting of parallel lines is defined by electron-beam lithography, and the exposed regions InGaAs fins are removed by RIE to form nanowire TFET arrays (step 4). These InGaAs TFET arrays are then contacted in the p^+ and n^+ regions by metal stacks (step 5), and electrical characterization is performed. Nanowire arrays with smaller ~30 nm diameters were also demonstrated using the same approach, showing a path to fabricate sub-50-nm NW TFET device arrays. Experiments are underway to
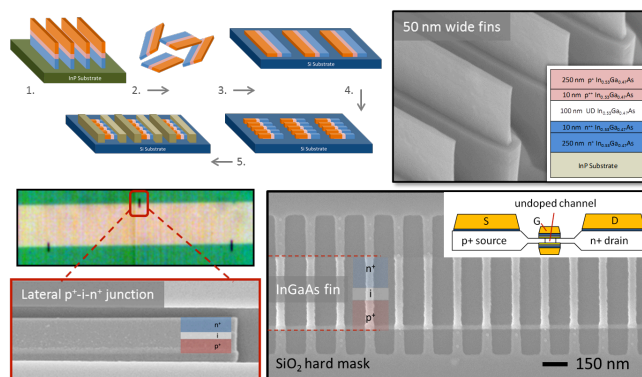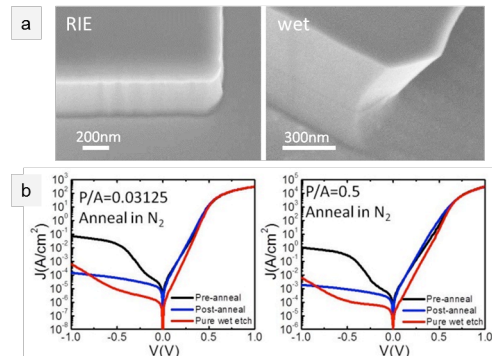

Figure 2. Scheme illustrating nanowire TFET fabrication process. FESEM and optical microscope images at step 1, 3, and 4.

optimize the electrical contact to the nanowires and characterize their electrical properties.

Publications and presentations since July 1, 2012:

- T. Mayer, S. Levin, Li, S. Datta, T. Morrow, Li, Kim, C. D. Keating, "Adding new functionality to Si CMOS via deterministic assembly," ECS Prime, Honolulu, HI, Oct. 2012.

Characterization of TFET interfaces – R. M. Wallace, J. Kim (UTD)

In collaboration with Dr. P. Laukkanen (Univ. Turku), the properties of the InAs(100)/crystalline oxide interface was investigated. The crystalline oxide on the InAs surface is formed *in situ* by removing an arsenic capping layer and exposing the sample to an oxygen environment at 350 °C. The growth of the crystalline oxide layer is then monitored using LEED and monochromatic X-ray photoelectron spectroscopy. Al_2O_3 was subsequently deposited on the oxidized surface to investigate the stability of crystalline oxide interface under ALD conditions. Oxidation at 350 °C with $p=7x10^{-6}$ mbar oxygen partial pressure results in (3x1)-O surface reconstruction. After exposing the sample to ALD reactor, the LEED pattern remained the same as after the oxidation process; however, after the first TMA pulse, the LEED pattern showed (1x1)-O unreconstructed surface, suggesting the interface is not stable upon TMA exposure.
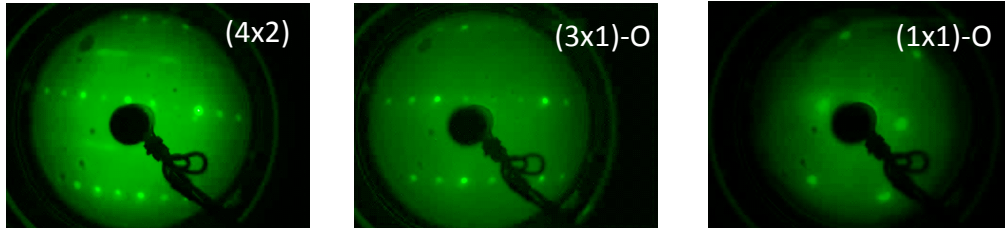

Figure 1. LEED patterns obtained on the decapped surface, oxidized and after the first TMA pulse exposure.

In collaboration with the Datta group at Penn State University, gate dielectric stack structures utilized for the III-V TFET project were investigated. These gate stack structures, grown at UT-Dallas and Penn State, include a nanolaminate Al_2O_3(10 Å)/HfO_2(4.5nm) stack on GaAsSb surfaces. $GaAs_{0.35}Sb_{0.65}$ wafers were utilized for these studies to provide initial surfaces. Figure 1 shows the Ga 2p, As 2p, Sb 3d and O 1s XPS spectra after citric acid etch followed by HCl-etch, exposure to the ALD reactor, 4 pulses of TMA pretreatment, subsequent Al_2O_3 deposition followed by an additional HfO_2 deposition to form the dielectric nanolaminate stack and forming gas anneal (FGA). Gallium, arsenic and antimony oxidation states detected after the chemical procedure are seen to decrease after TMA pulses pretreatment due to ALD "clean up" effect, however, the As-As, As$^-$ state were still detected at the interface. Upon FGA, oxidation states were seen to increase, most likely due to oxygen penetration during the anneal, suggesting that the forming gas may contain oxygen impurities. Further process refinements are being investigated as well as electrical characterization of the obtained gate stacks.
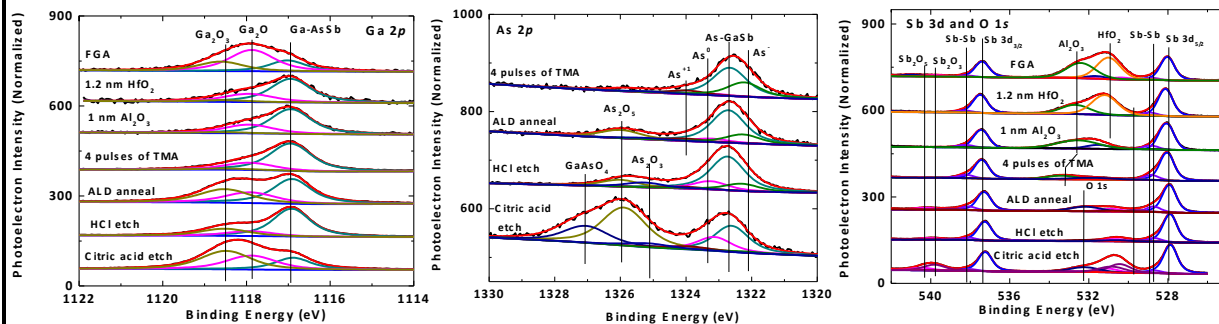

Figure 1. The Ga 2p, As 2p, Sb 3d and O 1s regions of the associated XPS spectra.

Futures plans on the III-V TFET interfaces structures involve further utilization of thermal oxides (arsenates and antimonites). To preserve the crystalline oxide interface, different types of high-k and deposition techniques are under investigation.

Publications and presentations (July 1 – October 31, 2012):
- D. Zhernokletov, S. McDonnell, H. Dong, B. Brennan, J. Kim, R. M. Wallace, "Half-cycle atomic layer deposition reaction studies of Al_2O_3/HfO_2 on the GaSb(001) surface," TECHCON 2012 Proceedings. SRC: P063738

Graphene nanoribbon TFETs – D. Jena, G. Xing (ND)

Since observing the NDR effect at room temperature in GNRs, we have developed a better understanding of the behavior by combined semi-analytical and numerical modeling. The GNRs were fabricated on CVD-grown graphene obtained from IBM, which allowed back- and side-gating. The NDR effect was observed only upon adding an electrolyte to the side gates, which effectively enhanced the side-gating efficiency creating p- and n-regions in the GNR.
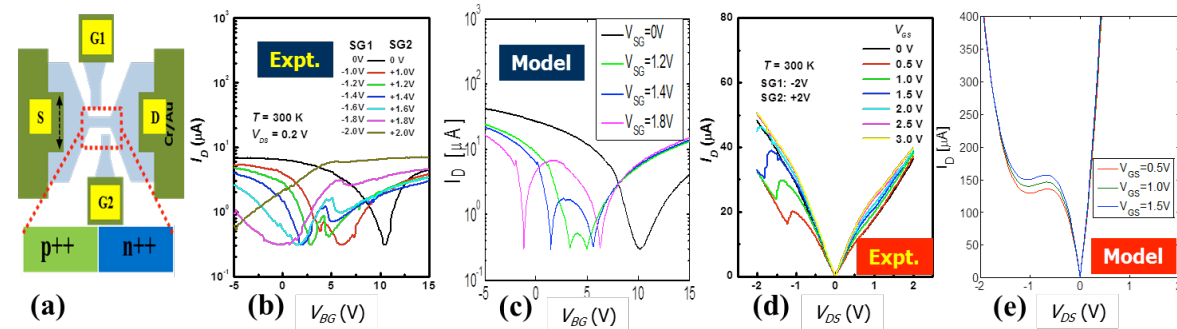

Figure 1: Side-gated GNR p-n junction that shows NDR effect at room temperature. A model was developed to explain the measured drain current controlled by the gate and the drain voltages for the device. The semi-analytical model shown here was put on a firmer basis with a NEGF-based simulation (not shown) performed in collaboration with Klimeck's group in Purdue.

Figure 1 shows the device, the measured data, and the results of the modeling. Based on this finding, the device can be made to work with solid dielectrics if the side-gating is much more efficient, or if we find a way to chemically dope the GNR into *p*- and *n*-regions. The other issue as is apparent from Figure 1(d) is that although the tunneling on-current with tunneling is appreciable (~1 mA/um), the device does not turn off at RT. This is expected since the bandgap of the GNR is too small for RT off-state operation. The experimental and modeling result thus offers two paths forward: (a) either make the GNRs much narrower to open up a substantial bandgap to turn the device off, and (b) find methods to chemically-dope or modulation dope the GNRs such that the side-gating is not necessary.
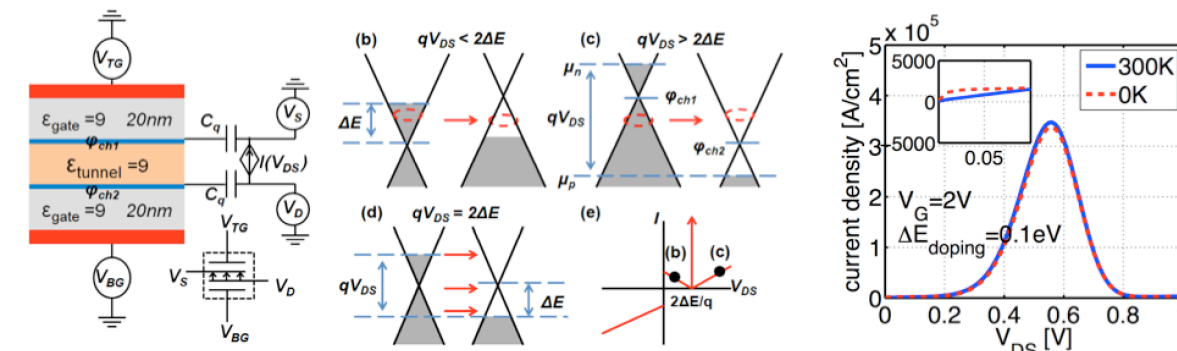

Figure 2: SymFET device concept, bandstructure under bias, and the calculated interlayer tunnelling current density at low temperature and at room temperature. Note that the interlayer tunnelling current is extremely high, approaching 0.5 MA/cm^2, which is a very attractive feature of the proposed device.

Based on our understanding of the transport properties of the two-terminal graphene-insulator-graphene (GIG) junctions, we developed a proposal for a gated structure. The transistor is called a SymFET since it takes advantage of the symmetry of the graphene bandstructure. By solving the electrostatic gate control problem, we have been able to calculate the expected device performance from a dc standpoint. The device will have a large on-current in a small *window* of drain *and* gate voltage biases, and the current will be low for all other bias conditions. The device performance will be robust to temperature variations, but stringent requirements on the rotational alignment of the two graphene layers are necessary. The device should be of interest for RF properties.
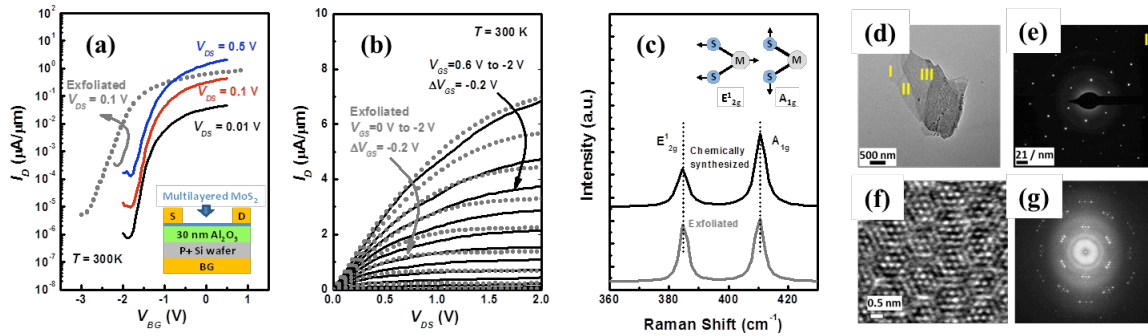
Figure 3: Long-channel FET characteristics of exfoliated and chemically synthesized MoS_2 FETs as a precursor to TFET realization with such layered 2D crystal semiconductors. We find that the chemically synthesized material is electronically and structurally equivalent to the naturally occurring material, which will help in systematic realization of controlled devices in the future.

Finally, based upon the challenges with GNR FETs, we have started investigating layered 2D crystal materials for possible TFET realization. Figure 3 shows normal FETs made with exfoliated, and chemically synthesized MoS_2 layers showing near identical switching and transport behaviors. Though MoS_2 has a large bandgap that will not enable high on-current TFETs, it will switch off as opposed to GNR TFETs. We plan to base our search for the optimal 2D materials for TFETs based on what we have learned from GNR TFETs for high on-currents in TFETs, and based on MoS_2-like materials for low-off currents.

Publications and presentations since July 1, 2012:

- R. Yan, Q. Zhang, O. A. Kirillov, W. Li, J. Basham, X. Liang, D. Jena, C. A. Richter, A. Seabaugh, D. J. Gundlach, H. Xing, and N. V. Nguyen, "Graphene as an electrode for directly observing hole injection from silicon to oxide," accepted, Semiconductor Interface Specialists Conference (SISC), Dec. 2012, San Diego, CA.
- B. Sensale-Rodriguez, Y. Lu, L. Barboni, F. Silveira, P. Fay, D. Jena, A. Seabaugh, and H. Xing, "Perspectives of TFETs for low power analog ICs," IEEE Subthreshold Microelectronics Conference, Oct. 2012, Waltham, MA.
- R. Yan, Q. Zhang, W. Li, I. Calizo, T. Shen, C. Richter, A. Hight-Walker, X. Liang, A. Seabaugh, H. Xing, D. Gundlach, and N. Nguyen, "Investigation of graphene-oxide-semiconductor band alignment by internal photoemission spectroscopy," International Symposium on Compound Semiconductors (ISCS), Aug. 2012, Santa Barbara, CA.
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- K. Xu, C. Zeng, Q. Zhang, R. Yan, P. Ye, K. Wang, A. Seabaugh, H. G. Xing, J. S. Suehle, C. A. Richter, D. J. Dunglach, and N. V. Nguyen, "Direct measurement of intrinsic Dirac point of graphene by cavity enhanced internal photoemission," submitted, *Nano Letters,* (2012).
- W. S. Hwang, M. Remskar, R. Yan, T. Kosel, J. K. Park, B. J. Cho, W. Haensch, H. G. Xing, A. Seabaugh, and D. Jena, "Comparative study of chemically synthesized and exfoliated multilayer MoS_2 field effect transistors," submitted, *Appl. Phys. Lett.,* 2012.

THEME 2: Nanomagnet Logic
Theme Leader: Wolfgang Porod
Email: porod@nd.edu

Theme 2 Executive Summary

Our NML research continues to address the key challenges needed to explore and demonstrate NML as a system component. Much of our previous work has concentrated on NML structures with in-plane magnetization, based on patterned thin-film magnetic materials. During the past year, we have begun to extend our work on structures with perpendicular (out-of-plane) magnetization, which we refer to as perpendicular magnetic logic (PML). Such PML devices can be clocked with a homogeneous and *global* magnetic field, which simplifies drive circuitry, and offers attractive architectural possibilities. This is a promising avenue of future research, based on lessons learned from our previous work.

Specifically, our research focused on three main themes, as described below.

Applications and architectures for NML: Our work suggests that the most significant impediment to NML-based, generalizable and compact logic is *not* the precessional period of a device's internal magnetic field – which limits the switching time of *all* spin-based devices to ~100 ps – but rather interconnect and signal routing. Given this, we are working to develop a new magnetic interconnect-based logic technology that is inspired by previous work, but where we seek to avoid the aforementioned challenges associated with in-plane NML – particularly with respect to signal routing and excessive numbers of nearest-neighbor interactions. Magnetic devices with perpendicular magnetic anisotropy (PMA) – referred to as perpendicular magnetic logic (PML) – offer a path toward circuits that (i) can be controlled with fine granularity, and (ii) do not suffer from the aforementioned signal routing issues.

Designs and prototypes of NML: To illustrate the potential benefits of the PMA-based device architecture, we have studied and benchmarked the specific case of an adder comprised of multiple layers of PML devices. Using the most recent NRI benchmarking effort as context (F=15 nm), a multi-layer, PML-based 32-bit adder could be ~100X smaller than a CMOS design. Moreover, a single, 32-bit add could be completed in the time required for just 33 magnet switching events. This makes the throughput per unit area of PML-based hardware highly competitive with respect to other NRI technologies, even without considering any benefits from inherent pipelining, further suggesting this as a promising avenue of future research.

Design and fabrication of energy efficient clocks for NML: A crucial element for NML is the clock, which provides the magnetic field needed to switch the individual nanomagnets. Reducing clocking energy for NML is an important goal of this research. We have fabricated and tested enhanced permeability dielectric (EPD) materials that, when deposited over the clocking structure and the nanomagnets, concentrates the field lines, hence lowering the current needed to switch the NML circuits. For stand-alone magnets, the EPD films have helped to lower the nulling clock field from 160 mT to 65 mT (~60% reduction). The same trend is seen in the sample of coupled magnets, where the nulling clock field decreases to 40 mT from 160 mT, a 75% reduction. This indicates that EPD films may not only reduce the switching fields of magnets, but also modify the coupling field between them.

Applications & architectures for NML – G. Csaba, S. Hu, P. Kogge, M. Niemier, W. Porod (ND)

Summary of in-plane NML work: Our study of field-clocked NML devices with in-plane magnetization states suggests that NML could deliver energy savings when compared to CMOS hardware equivalents at iso-performance. However, said gains are typically derived from specialized, highly pipelined/parallel architectures, and amortization of clock energy over specific sub-ensembles.

Our work suggests that the most significant impediment to NML-based, generalizable and compact logic is *not* the precessional period of a device's internal magnetic field – which limits the switching time of *all* spin-based devices to ~100 ps – but rather interconnect and signal routing. **(1)** Technologically, NML is capable of performing more complex logic operations (*e.g.,* majority voting operations) with just a single magnet-switching event. However, as local signal routing is also dependent on magnet-to-magnet fringing field interactions, the time required to move a signal from one gate output to another gate input could be more than an order of magnitude higher than the gate delay itself. **(2)** Furthermore, the fringing fields from one device that set the state of another (for either a logic or interconnect operation) are *in-plane*. This further complicates local signal routing. For example, wire crossings that are common-place in CMOS (because of multiple levels/planes of metal) have proven to be challenging to duplicate with in-plane magnetic logic devices. **(3)** Finally, in order to avoid signal back propagation, multi-phase clock structures are required. This necessitates that signal routing occur *at the granularity of the clock* and makes local, bi-directional signal flow inefficient.

Future directions: Given this, we are working to develop a new magnetic interconnect-based logic technology that is inspired by previous work, but where we seek to avoid the aforementioned challenges associated with in-plane NML – particularly with respect to signal routing and excessive numbers of nearest-neighbor interactions. Magnetic devices with perpendicular magnetic anisotropy (PMA) – referred to as perpendicular magnetic logic (PML) – offer a path toward circuits that (i) can be controlled with fine granularity, and (ii) do not suffer from the aforementioned signal routing issues.

Architecturally, our work suggests that the advantages of perpendicular media over in-plane media are many-fold. Notably, **(1)** PML devices are more amenable to voltage controlled clocking – *i.e.,* via multiferroic materials, piezoelectric materials, or the spin Hall effect – which represents a path to fine-grained, bi-directional dataflow *and* low energy clocking. (Moreover, techniques such as ion milling can also be used to define a nucleation site within a device and define dataflow directionality without using *any* multi-phase clocking.) **(2)** The use of devices with PMA opens the door to multiple layers of metallic devices that couple in a third dimension. This not only reduces circuit area (see next page), but also leads to stronger device-to-device coupling, which will reduce error rates. **(3)** PML offers the ability to create circuits with a high fan-in – which can (i) reduce the number of devices required to perform a given logic function (see adder example on the next page). **(4)** Finally, with respect to signal routing, PML enables the use of long domain walls for information transfer. Per experiments with TU-Munich, CoPt domain walls can cross above/below one other. Stray fields from one strip do not unduly affect the other. *As such, multi-level wire crossings are possible.* Moreover propagating domain walls in magnetic stripes that reside either above or below PML devices can serve as a fast, medium/global-scale interconnect when considering signal routing to PML-based logic gates. Many neighbor-to-neighbor interactions are not needed.

Fault tolerant architectures: A challenge associated with processing information using devices that communicate via magnetic interconnect (or with any scaled, emerging technology) is the possibility of higher bit error rates than we have become accustomed to with CMOS-based hardware. As such, we have begun a study of stochastic computing architectures that (i) are particularly well suited to streaming dataflow associated with many spin-based devices, (ii) are capable of tolerating errors at the bit level, and (iii) require minimal device hardware. More specifically, with *stochastic logic*, rather than transforming an absolute input into an absolute output (*e.g.,* via a Boolean logic gate), circuits transform "probability values into probability values" [13]. In stochastic computation, the value of a signal is interpreted as a probability regardless of normal or faulty conditions. Stochastic computation (suitable for image processing, etc.) is naturally fault tolerant as a small number of bit flips only result in small deviations from the desired value. While computation time could increase as the precision of stochastic values increases [14], given inherently pipelined, streaming dataflow, more efficient implementations of stochastic computing architectures should be possible.

Publications and presentations since July 1, 2012:

- J. Kiermaier, S. Breitkreutz, I. Eichwald, J. Engelstädter, X. Ju, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Information transport in field-coupled nanomagnetic logic devices," submitted, 12th joint Intermag/MMM, Jan. 2013, Chicago, IL.
- I. Eichwald, J. Wu, J. Kiermaier, S. Breitzkreutz, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Towards a signal crossing in 2-level nanomagnetic logic," submitted, 12th joint Intermag/MMM, January 2013, Chicago, IL.
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- I. Palit, X. S. Hu, J. Nahas, and M. Niemier, "Systematic design of nanomagnet logic circuits," accepted, Design Automation and Test Europe (DATE), Mar. 2013, Grenoble, France.

Designs & prototypes of NML circuits & reduced energy, latency & area – G. Bernstein, G. Csaba, S. Hu, J. Nahas, M. Niemier, W. Porod (ND)

To illustrate the potential benefits of the PMA-based device architecture described on the previous page, we consider how an adder comprised of multiple layers of PML devices might fare given the context of the most recent NRI benchmarking effort. The design (Fig. 1) is based on the two-majority gate threshold adder. The carry output (C_{out}) can be determined simply by performing typical majority voting functions $M(A,B,C_{in})$. The sum output can then be realized by a 5-input majority voter: $M(A,B,C_{in},C'_{out},C'_{out})$. With in-plane nanomagnet logic, the single domain limit necessitates that device footprint be relatively small which limits fan-in. PML devices can not only be larger, but can also couple in multiple dimensions. Note that in Fig. 1, the AF-coupling between the A, B, and C inputs and the C_{out} target would result in the generation of C'_{out}. Additionally, by placing the Sum target *above* A, B, C_{in}, and C'_{out}, the correct signal values will be fed to Sum. (The Sum target is sized such that the fringing field magnitude from C_{out} is two times that of A, B, or C_{in}.) As such, a full adder can be realized with just five devices.

Using the most recent NRI benchmarking effort as context (F=15 nm), a multi-layer, PML-based 32-bit adder could be ~100X smaller than a CMOS design. Moreover, a single, 32-bit add could be completed in the time required for just 33 magnet switching events. Per Fig. 2, this makes the throughput per unit area of pNML-based hardware highly competitive with respect to other NRI technologies (without considering any benefits from inherent pipelining). This would allow PML to approach 20 PIOPS/cm^2 (superior to any other benchmarked device) with a peak power of just 2.6W. Note that this

Figure 1: Schematic of integrated adder cell using PML. (Assuming '0' maps to ↑ and '1' maps to ↓, the magnetization state for input combination A=1, B=0, C_{in}=1 is shown.) Note that the C_{out} magnet (with a complemented value) could move a signal up in the vertical direction to another level, or within the same plane.

Figure 2: **(a)** Schematic showing concatenated bits. In a pipelined circuit, a new result could be completed every 2 clock cycles after the pipeline is filled; **(b)** Multi-layer PML circuits offer the promise of high computational density. Note that power projections are based on existing NRI data for magnetostrictive switching.

assumes 5 ns clock pulses! Further, while not discussed here due to space limitations, domain walls in magnetic stripes above or below input magnets could also be used to route signals.
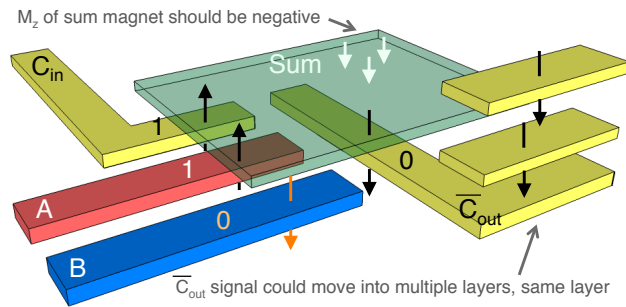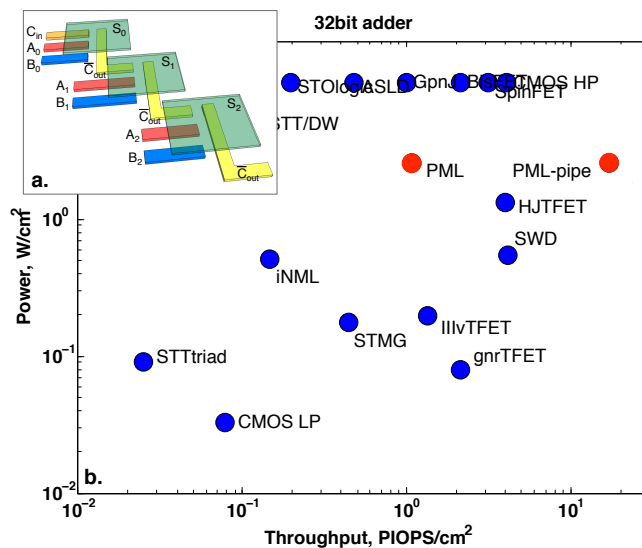
Publications and presentations since July 1, 2012:
- I. Eichwald, A. Bartel, J. Kiermaier, S. Breitkreutz, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Nanomagnetic Logic: error-free, directed signal transmission by an inverter chain," accepted, *IEEE Trans. on Magnetics.*
- S. Breitkreutz , J. Kiermaier, I. Eichwald, X. Ju, G. Csaba, D. Schmitt- Landsiedel, and M. Becherer, "Majority gate for nanomagnetic logic with perpendicular magnetic anisotropy," *accepted, IEEE Trans. on Magnetics.*
- S. Breitkreutz, J. Kiermaier, I. Eichwald, C. Hildbrand, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Experimental demonstration of a 1-bit full adder in perpendicular nanomagnetic logic,"

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- S. Breitkreutz, J. Kiermaier, I. Eichwald, X. Ju, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Investigations on nanomagnet logic by experiment-based compact modeling," accepted, *Nanoelectronic Device Applications Handbook* eds: Morris / Iniewski.
- E. Varga, M. T. Niemier, G. Csaba, G. H. Bernstein, and W. Porod, "Experimental realization of a nanomagnet full adder using slanted-edge input magnets," accepted, Joint MMM/Intermag Conference, Jan. 2013, Chicago, IL.
- E. Varga, M. T. Niemier, G. Csaba, G. H. Bernstein, and W. Porod, "Experimental realization of a nanomagnet full adder using slanted-edge magnets," submitted, *IEEE Trans. on Magnetics*.
- M. A. Siddiq, M. Niemier, G. Csaba, X. S. Hu, W. Porod, and G.H. Bernstein, "Demonstration of field coupled input scheme on line of nanomagnets," submitted, *IEEE Trans. on Magnetics*.
- H. Dey, G. Csaba, X. S. Hu, M. Niemier, G. Bernstein, and W. Porod, "Switching behavior of sharply pointed nanomagnets for logic applications," under review, *IEEE Trans. on Magnetics*.
- M. A. Siddiq, G. H. Bernstein, M. T. Niemier, X. S. Hu, G. Csaba, and W. Porod, "Demonstration of field-coupled input scheme on line of nanomagnets," accepted, Joint MMM/Intermag Conference, Jan. 2013, Chicago, IL.
- M. A. Siddiq, M. T. Niemier, G. H. Bernstein, W. Porod, and X. S. Hu, "A field coupled electrical input for nanomagnet logic," submitted, *IEEE Trans. on Nanotechnology*.
- S. Kurtz, A. Dingler, M. Niemier, X. S. Hu, G. Csaba, J. Nahas, W. Porod, and G. Bernstein, "Preserving steady state non-volatility in nanomagnet logic circuits," TECHCON Sept. 2012, Austin, TX.
- F. Shah, G. Csaba, K. Butler, and G. Bernstein, "Closely spaced nanomagnets by dual e-beam exposure for low-energy NML," submitted, *J. Appl. Phys.,* 2012.

Design & fabrication of energy efficient clocks for NML – G. Bernstein, S. Hu, J. Nahas, M. Niemier, W. Porod (ND)

With respect to field-based clocking of in-plane nanomagnet logic devices, we have proposed the use of enhanced permeability dielectrics (EPD) films to reduce power consumption in line clocked NML circuits. EPDs with embedded magnetic nano-particles (e.g. CoFe particles 2-5 nm in diameter) could increase absolute permeability ($\mu=\mu_o x \mu_r$) by increasing the relative permeability μ_r and reduce Ohmic losses by μ_r^2.

We can now report clock field requirements to change the state of *coupled magnets* with and without EPD films. As samples cannot be interrogated with magnetic force microscopy, we need another method for determining clock field requirements to induce anti-ferromagnetic ordering in pairs of devices that are initially aligned in parallel. In NML, a hard-axis directed clock field places magnets into a metastable state (i.e., set M_y =0). Upon field removal, magnets relax to the computational ground state. M_y vs. H_x curves (where x is the hard axis and y is the easy axis) provide the most relevant information for NML operation; it is also straightforward to measure, as the M_y component comes solely from the nanomagnets, and the EPD films provide no magnetization component with respect to the vertical direction of the applied field.

All M_y vs. H_x curves are measured as described below. First, we magnetize a sample along the easy axis (y). Then, starting from zero, we gradually apply an external field along the hard axis of the magnets along the positive x-direction. Then we sweep the field in the opposite direction. M_y is monitored using the vector coils of the VSM. To begin, consider a standalone case without EPDs (Fig. 1a, Fig. 2) where, after the array is magnetized along the y axis, the magnets have a strong M_y component (stage A); with an increasing hard-axis field in the positive x-direction, M_y gradually decreases, and when the field reaches 160 mT, all of the magnetization points right, and M_y =0 (stage B). When the field sweeps back to zero, the magnets turn up or down randomly, so M_y remains at zero (stage C). Finally, when the field is increased in the negative x-direction, the magnetization states of the devices in the array point left, and M_y stays at zero.

The switching process of the coupled magnets without EPDs (Fig. 1b) is similar to that of the standalone case. However, the coupling field between the two magnets is another field component driving them toward the hard-axis direction, and reduces their net switching fields. This is reflected in the slopes of the curves. When the external field is zero (stage C), the magnetization of the two coupled magnets are aligned anti-ferromagnetically. Fig. 2 shows the experimental curves for the standalone and coupled magnets, where the curves are normalized for comparison. The experimental data agree well with the simulations regarding the clock fields at which the magnetization goes to zero (*i.e.,* the minimum field required to null the magnets), as well as the slopes of the curves.

After the samples are covered with EPD films, the nanomagnets switch at much lower fields. Fig. 3 shows experimental M_y vs. H_x curves for both standalone (Fig. 3a) and coupled magnets (Fig. 3b). For the standalone case, the EPD films have helped to lower the nulling clock field from 160 mT to 65 mT (~60% reduction). Note that the remanent values of M_y are the same before and after the deposition of the EPD films, which echoes previous experiments. This confirms that EPDs do not add any residual background magnetic bias to the NML switching characteristics.

The same trend is seen in the sample of coupled magnets, where the nulling clock field decreases to 40 mT from 160 mT, a 75% reduction. This indicates that EPD films may not only reduce the switching fields of magnets, but also modify the coupling field between them. Work to understand the effect of EPD films on the coupling fields is in progress.
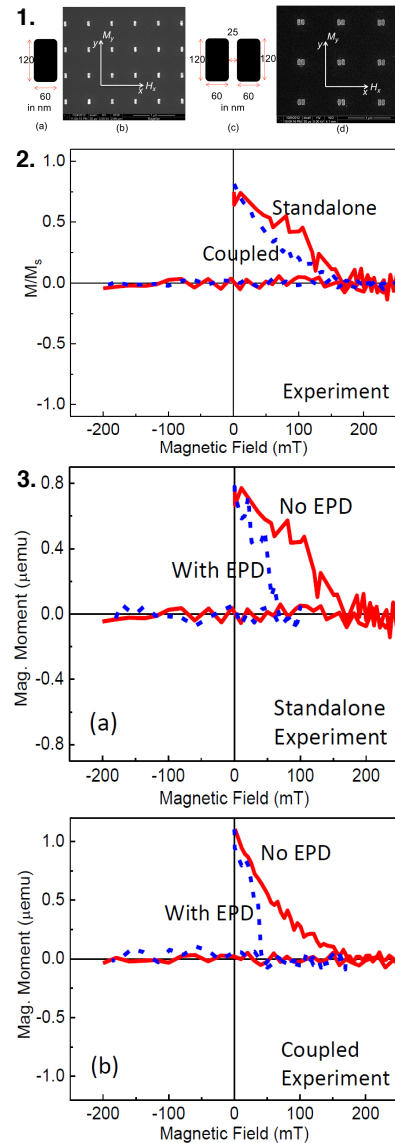
Publications and presentations since July 1, 2012:

- E. Varga, G. Csaba, G. H. Bernstein, and W. Porod, "Domain-wall assisted switching of single-domain nanomagnets," accepted, *IEEE Trans. on Magnetics.*
- P. Li, G. Csaba, V. K. Sankar, X. S. Hu, M. Niemier, W. Porod, G. H. Bernstein, "Paths to clock power reduction via high permeability dielectrics for nanomagnet logic circuits," accepted, Joint MMM/Intermag Conference, Jan. 2013, Chicago, IL.
- P. Li, G. Csaba, V. K. Sankar, X. Ju, E. Varga, P. Lugli, X. P. Li, G. Csaba, M. Niemier, X. S. Hu, J. Nahas, W. Porod, and G. H. Bernstein, "Power reduction in nanomagnet logic using high permeability dielectrics," submitted, *J. Appl. Phys.*
- M. Siddiq, G. Bernstein, M. Niemier, X. S. Hu, G. Csaba, and W. Porod, "Field estimation of a NML clock line using switching statistics of different aspect ratio nanomagnets," accepted, Joint MMM/Intermag Conference, Jan. 2013, Chicago, IL.

THEME 3: Architectures and Benchmarking
Theme Leaders: Alan Seabaugh and Wolfgang Porod
Email: seabaugh.1@nd.edu, porod@nd.edu

Theme 3 Executive Summary:

The benchmarking inputs for both TFET and NML technologies were continued, this time within the framework of the methodology led by Drs. Dmitri Nikonov and Ian Young at Intel. The NML benchmarking effort comprises the work at Notre Dame and UC Berkeley, while the TFET benchmarking includes Notre Dame, Penn State, and Purdue. The results of this effort were presented at the *NRI Architectures & Device Benchmarking Workshop*, which was held on August 14 at Notre Dame, immediately prior to the MIND Annual Review. The MIND team took the lead in organizing this workshop where all NRI technologies were featured.

Architectures and benchmarking of TFET and NML – S. Hu, P. Kogge, J. Nahas, M. Niemier, W. Porod, A. Seabaugh (ND)

For the TFET benchmarking, simulations were provide on four transistors with a gate length of 15 nm: (1) a double-gate *p-i-n* planar nTFET with an InAs channel, (2) a double-gate *p-i-n* planar nTFET with a heterojunction *p*-GaSb source and an InAs channel, (3) a p-GaSb/n-InAs channel gate-all-around nanowire geometry, and (4) a graphene nanoribbon TFET.   Penn State also provide a TCAD model to project the performance of 15 nm CMOS.

The NML benchmarking effort comprises the work at ND and also at UC Berkeley (Bokor and Salahuddin groups). The ND team worked closely with Drs. Dmitri Nikonov and Ian Young on applying their benchmarking methodology to the specifics of NML technology. Several conference calls were held during early 2012, and the results of this effort were presented at the *NRI Architectures & Device Benchmarking Workshop,* which was held at Notre Dame during August.

The Notre Dame team also took the lead in organizing the *NRI Architectures & Device Benchmarking Workshop*, which was held on August 14 at Notre Dame, immediately prior to the MIND Annual Review. All technologies included in NRI 1.5 were presented, as well as a summary read-out of the overall Intel-led effort, which was presented by Dr. Dmitri Nikonov.

Publications and presentations since July 1, 2012:
None to report.

Publications and patents

	Q1, 2	Q3, 4	Total
Journal Papers	**15**	**19**	**34**
Conference Papers	**38**	**19**	**57**
Patents	**0**	**1**	**1**

List of Journal Publications for this 6 months

Project # 1: Modeling and analysis of tunnel transistors with NEMO/OMEN
None to report.

Project # 2: Heterojunction *p-n* tunnel field-effect transistors
- Q. Liu, L. Dong, Y. Liu, R. Gordon, P. D. Ye, P. Fay, and A. Seabaugh, "Frequency response of LaAlO$_3$/SrTiO$_3$ all-oxide field-effect transistors," *Solid-State Electronics,* 76, 2012, 1-4.
- Q. Zhang, R. Li, R. Yan, T. Kosel, H. G. Xing, A. Seabaugh, K. Xu, O. A. Kirillov, D. J. Gundlach, C. A. Richter, and N. V. Nguyen, "A unique photoemission method to measure semiconductor heterojunction band offsets," submitted, *Appl. Phys. Lett.,* 2012.

Project # 3: Heterojunction *p-i-n* tunnel transistor logic and architectures
- D. K. Mohata, R. Bijesh, T. Mayer, J. Fastenau, D. Lubyshev, A. K. Liu, and S. Datta, "Barrier engineered arsenide-antimonide hetero-junction tunnel FETs with enhanced drive current," *IEEE Electron Dev. Lett.,* vol. 33, no. 11, pp. 1568-1570, 2012.
- Y. Zhu, N. Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M. K. Hudait, "Structural properties and band offset determination of p-channel mixed As/Sb type-II staggered gap tunnel field-effect transistor structure," *Appl. Phys. Lett.* 101, 112106, 2012.

Project # 4: Nanofabrication platform for one-dimensional nanowire tunnel transistors
None to report.

Project # 5: Characterization of tunnel field-effect transistor interfaces
None to report.

Project # 6: Graphene nanoribbon tunnel field-effect transistors
- R. Yan, Q. Zhang, O. A. Kirillov, W. Li, J. Basham, A. Boosalis, X. Liang, D. Jena, C. Richter, A. Seabaugh, D. Gundlach, H. G. Xing, and N. Nguyen, "Graphene as transparent electrode for direct observation of hole photoemission from silicon to oxide," submitted, *Nano Letters,* (2012).
- R. Yan, S. Bertolazzi, Jacopo Brivio, T. Fang, A. Konar, A. G. Birdwell, N. V. Nguyen, A. Kis, D. Jena, and H. G. Xing, "Raman and photoluminescence study of dielectric and thermal effects on atomically thin MoS$_2$." submitted, *Appl. Phys. Lett.,* (2012).
- K. Xu, C. Zeng, Q. Zhang, R. Yan, P. Ye, K. Wang, A. Seabaugh, H. G. Xing, J. S. Suehle, C. A. Richter, D. J. Dunglach, and N. V. Nguyen, "Direct measurement of intrinsic Dirac point of graphene by cavity enhanced internal photoemission," submitted, *Nano Letters,* (2012).
- W. S. Hwang, M. Remskar, R. Yan, T. Kosel, J. K. Park, B. J. Cho, W. Haensch, H. G. Xing, A. Seabaugh, and D. Jena, "Comparative study of chemically synthesized and exfoliated multilayer MoS$_2$ field effect transistors," submitted, *Appl. Phys. Lett.,* 2012.

Project # 7: Applications and architectures for nanomagnet logic
- X. Ju, M. Niemier, M. Becherer, W. Porod, P. Lugli, and G. Csaba, "Systolic pattern matching hardware with out-of-plane nanomagnet logic devices," accepted, *IEEE Trans. on Nanotechnology*.

Project # 8: Designs and prototypes of NML circuits with reduced energy, latency, and area

- I. Eichwald, A. Bartel, J. Kiermaier, S. Breitkreutz, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Nanomagnetic Logic: error-free, directed signal transmission by an inverter chain," accepted, *IEEE Trans. on Magnetics.*
- S. Breitkreutz , J. Kiermaier, I. Eichwald, X. Ju, G. Csaba, D. Schmitt- Landsiedel, and M. Becherer, "Majority gate for nanomagnetic logic with perpendicular magnetic anisotropy," *accepted, IEEE Trans. on Magnetics.*
- S. Breitkreutz, J. Kiermaier, I. Eichwald, X. Ju, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Investigations on nanomagnet logic by experiment-based compact modeling," accepted, *Nanoelectronic Device Applications Handbook* eds: Morris / Iniewski.
- E. Varga, M. T. Niemier, G. Csaba, G. H. Bernstein, and W. Porod, "Experimental realization of a nanomagnet full adder using slanted-edge magnets," submitted, *IEEE Trans. on Magnetics*.
- M. A. Siddiq, M. Niemier, G. Csaba, X. S. Hu, W. Porod, and G.H. Bernstein, "Demonstration of field coupled input scheme on line of nanomagnets," submitted, *IEEE Trans. on Magnetics*.
- H. Dey, G. Csaba, X. S. Hu, M. Niemier, G. Bernstein, and W. Porod, "Switching behavior of sharply pointed nanomagnets for logic applications," under review, *IEEE Trans. on Magnetics*.
- M. A. Siddiq, M. T. Niemier, G. H. Bernstein, W. Porod, and X. S. Hu, "A field coupled electrical input for nanomagnet logic," submitted, *IEEE Trans. on Nanotechnology*.
- F. Shah, G. Csaba, K. Butler, and G. Bernstein, "Closely spaced nanomagnets by dual e-beam exposure for low-energy NML," submitted, *J. Appl. Phys.,* 2012.

Project # 9: Design and fabrication of energy efficient clocks for NML

- E. Varga, G. Csaba, G. H. Bernstein, and W. Porod, "Domain-wall assisted switching of single-domain nanomagnets," accepted, *IEEE Trans. on Magnetics.*
- P. Li, G. Csaba, V. K. Sankar, X. Ju, E. Varga, P. Lugli, X. P. Li, G. Csaba, M. Niemier, X. S. Hu, J. Nahas, W. Porod, and G. H. Bernstein, "Power reduction in nanomagnet logic using high permeability dielectrics," submitted, *J. Appl. Phys.*

Project # 10: Architectures and benchmarking of TFET and NML technologies
None to report.

List of Conference Publications for this 6 months

Project # 1: Modeling and analysis of tunnel transistors with NEMO/OMEN
None to report.

Project # 2: Heterojunction *p-n* tunnel field-effect transistors

- A. Seabaugh, "Tunnel field-effect transistor perspective," invited, International Symposium on Compound Semiconductors, August 2012, Santa Barbara, CA.
- Q. Zhang, R. Li, T. Kosel, H. Xing, A. Seabaugh, K. Xu, O. A. Kirillov, C. A. Richter, D. J. Gundlach, and N. V. Nguyen, "Band offsets of Al_2O_3 on InAs/AlGaSb heterojunction measured by internal photoemission," accepted poster, IEEE Semiconductor Interface Specialists Conference, Dec. 2012, San Diego, CA.
- M. I. Shams, Y. Xie, Y. Lu, and P. Fay, "An accurate interband tunneling model for InAs/GaSb heterostructure devices," International Symposium on Compound Semiconductors, Santa Barbara, CA, Aug. 2012, Santa Barbara, CA.

Project # 3: Heterojunction *p-i-n* tunnel transistor logic and architectures

- R. Mukundrajan, M. Cotter, V. Saripalli, M. J. Irwin, S. Datta, and V. Narayanan, "Ultra low power circuit design using tunnel FETs," IEEE Computer Society Annual Symposium on VLSI, Aug. 2012, Amherst, MA.
- E. Kultursay, K. Swaminathan , V. Saripalli, S. Datta , V. Narayanan, and M. Kandemir, "Performance enhancement under power constraints using heterogeneous CMOS-TFET multicores," accepted, IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis, Oct. 2012, Tampere, Finland.

Project # 4: Nanofabrication platform for one-dimensional nanowire tunnel transistors
- T. Mayer, S. Levin, Li, S. Datta, T. Morrow, Li, Kim, C. D. Keating, "Adding new functionality to Si CMOS via deterministic assembly," ECS Prime, Honolulu, HI, Oct. 2012.

Project # 5: Characterization of tunnel field-effect transistor interfaces
- D. Zhernokletov, S. McDonnell, H. Dong, B. Brennan, J. Kim, R. M. Wallace, "Half-cycle atomic layer deposition reaction studies of Al_2O_3/HfO_2 on the GaSb(001) surface," TECHCON 2012 Proceedings. SRC: P063738

Project # 6: Graphene nanoribbon tunnel field-effect transistors
- R. Yan, Q. Zhang, O. A. Kirillov, W. Li, J. Basham, X. Liang, D. Jena, C. A. Richter, A. Seabaugh, D. J. Gundlach, H. Xing, and N. V. Nguyen, "Graphene as an electrode for directly observing hole injection from silicon to oxide," accepted, Semiconductor Interface Specialists Conference (SISC), Dec. 2012, San Diego, CA.
- B. Sensale-Rodriguez, Y. Lu, L. Barboni, F. Silveira, P. Fay, D. Jena, A. Seabaugh, and H. Xing, "Perspectives of TFETs for low power analog ICs," IEEE Subthreshold Microelectronics Conference, Oct. 2012, Waltham, MA.
- R. Yan, Q. Zhang, W. Li, I. Calizo, T. Shen, C. Richter, A. Hight-Walker, X. Liang, A. Seabaugh, H. Xing, D. Gundlach, and N. Nguyen, "Investigation of graphene-oxide-semiconductor band alignment by internal photoemission spectroscopy," International Symposium on Compound Semiconductors (ISCS), Aug. 2012, Santa Barbara, CA.

Project # 7: Applications and architectures for nanomagnet logic
- J. Kiermaier, S. Breitkreutz, I. Eichwald, J. Engelstädter, X. Ju, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Information transport in field-coupled nanomagnetic logic devices," submitted, 12th joint Intermag/MMM, Jan. 2013, Chicago, IL.
- I. Eichwald, J. Wu, J. Kiermaier, S. Breitzkreutz, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Towards a signal crossing in 2-level nanomagnetic logic," submitted, 12th joint Intermag/MMM, Jan. 2013, Chicago, IL.
- I. Palit, X. S. Hu, J. Nahas, and M. Niemier, "Systematic design of nanomagnet logic circuits," accepted, Design Automation and Test Europe (DATE), Mar. 2013, Grenoble, France.

Project # 8: Designs and prototypes of NML circuits with reduced energy, latency, and area
- S. Breitkreutz, J. Kiermaier, I. Eichwald, C. Hildbrand, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Experimental demonstration of a 1-bit full adder in perpendicular nanomagnetic logic," submitted, 12th joint Intermag/MMM, Jan. 2013, Chicago, IL.
- E. Varga, M. T. Niemier, G. Csaba, G. H. Bernstein, and W. Porod, "Experimental realization of a nanomagnet full adder using slanted-edge input magnets," accepted, Joint MMM/Intermag Conference, Jan. 2013, Chicago, IL.
- M. A. Siddiq, G. H. Bernstein, M. T. Niemier, X. S. Hu, G. Csaba, and W. Porod, "Demonstration of field-coupled input scheme on line of nanomagnets," accepted, Joint MMM/Intermag Conference, Jan. 2013, Chicago, IL.
- S. Kurtz, A. Dingler, M. Niemier, X. S. Hu, G. Csaba, J. Nahas, W. Porod, and G. Bernstein, "Preserving steady state non-volatility in nanomagnet logic circuits," TECHCON Sept. 2012, Austin, TX.

Project # 9: Design and fabrication of energy efficient clocks for NML
- P. Li, G. Csaba, V. K. Sankar, X. S. Hu, M. Niemier, W. Porod, G. H. Bernstein, "Paths to clock power reduction via high permeability dielectrics for nanomagnet logic circuits," accepted, Joint MMM/Intermag Conference, Jan. 2013, Chicago, IL.
- M. Siddiq, G. Bernstein, M. Niemier, X. S. Hu, G. Csaba, and W. Porod, "Field estimation of a NML clock line using switching statistics of different aspect ratio nanomagnets," accepted, Joint MMM/Intermag Conference, Jan. 2013, Chicago, IL.

Project # 10: Architectures and benchmarking of TFET and NML technologies
None to report.

PUBLICATIONS AND PATENTS

Top 5-10 Journal Publications for the Duration of the Center's Operation

Top 11 journal publications in MIND (according to Web of Science)

1. Mobility in semiconducting graphene nanoribbons: Phonon, impurity, and edge roughness scattering
Author(s): Fang Tian; Konar Aniruddha; Xing Huili; Jena Debdeep
Source: PHYSICAL REVIEW B Volume: **78** Issue: **20**   Article Number: **205403** DOI: **10.1103/PhysRevB.78.205403** Published: **NOV 2008** Times Cited: **62** (from All Databases)

2. Graphene Nanoribbon Tunnel Transistors
Author(s): Zhang Qin; Fang Tian; Xing Huili; Seabaugh Alan; Jena Debdeep
Source: IEEE ELECTRON DEVICE LETTERS Volume: **29** Issue: **12** Pages: **1344-1346** DOI: **10.1109/LED.2008.2005650** Published: **DEC 2008** Times Cited: **53** (from All Databases)

3. Programmed Assembly of DNA-Coated Nanowire Devices
Author(s): Morrow Thomas J.; Li Mingwei; Kim Jaekyun; Mayer Theresa; Keating CD
Source: SCIENCE Volume: **323** Issue: **5912** Pages: **352-352** DOI: **10.1126/science.1165921**
Published: **JAN 16 2009** Times Cited: **48** (from All Databases)

4. Atomistic Full-Band Design Study of InAs Band-to-Band Tunneling Field-Effect Transistors
Author(s): Luisier Mathieu; Klimeck Gerhard
Source: IEEE ELECTRON DEVICE LETTERS Volume: **30** Issue: **6** Pages: **602-604**
DOI: **10.1109/LED.2009.2020442** Published: **JUN 2009** Times Cited: **34** (from All Databases)

5. Atomistic Full-Band Simulations of Silicon Nanowire Transistors: Effects of Electron-Phonon Scattering
Author(s): Luisier Mathieu; Klimeck Gerhard
Source: PHYSICAL REVIEW B Volume: **80** Issue: **15**   Article Number: **155430**
DOI: **10.1103/PhysRevB.80.155430** Published: **OCT 2009** Times Cited: **33** (from All Databases)

6. Ultrafast Transient Absorption Microscopy Studies of Carrier Dynamics in Epitaxial Graphene
Author(s): Huang Libai; Hartland Gregory V.; Chu Li-Qiang; Luxmi; Feenstra R. Lian Chuanxin, Tahy Kristof, Xing Grace
Source: NANO LETTERS Volume: **10** Issue: **4** Pages: **1308-1313** DOI: **10.1021/nl904106t**
Published: **APR 2010** Times Cited: **31** (from All Databases)

7. Effect of high-kappa gate dielectrics on charge transport in graphene-based field effect transistors_
Author(s): Konar Aniruddha; Fang Tian; Jena Debdeep
Source: PHYSICAL REVIEW B Volume: **82** Issue: **11**   Article Number: **115452** DOI: **10.1103/PhysRevB.82.115452** Published: **SEP 29 2010** Times Cited: **25** (from All Databases)

8. Zener tunneling in semiconducting nanotube and graphene nanoribbon p-n junctions _
Author(s): Jena Debdeep; Fang Tian; Zhang Qin; Xing Huili
Source: APPLIED PHYSICS LETTERS Volume: **93** Issue: **11**   Article Number: **112106** DOI: **10.1063/1.2983744** Published: **SEP 15 2008** Times Cited: **24** (from All Databases)

9. Low-Voltage Tunnel Transistors for Beyond CMOS Logic
Author(s): Seabaugh Alan C.; Zhang Qin
Source: PROCEEDINGS OF THE IEEE Volume: **98** Issue: **12** Pages: **2095-2110** DOI: **10.1109/JPROC.2010.2070470** Published: **DEC 2010** Times Cited: **24** (from All Databases)

10. In Situ Axially Doped n-Channel Silicon Nanowire Field-Effect Transistors
Author(s): Ho Tsung-ta; Wang Yanfeng; Eichfeld Sarah; Lew Kok-Keong; Liu Bangzhi; Mohney Suzanne; Redwing Joan; Mayer Theresa Source: NANO LETTERS Volume: **8** Issue: **12** Pages: **4359-4364** DOI: **10.1021/nl8022059** Published: **DEC 2008** Times Cited: **22** (from All Databases)

11. On-Chip Clocking for Nanomagnet Logic Devices_
Author(s): Alam Tanvir; Siddiq Jafar; Bernstein Gary H.; Niemier Michael; Porod Wolfgang; Hu Sharon
Source: IEEE TRANSACTIONS ON NANOTECHNOLOGY Volume: **9** Issue: **3** Pages: **348-351**
 DOI: **10.1109/TNANO.2010.2041248** Published: **MAY 2010** Times Cited: **20** (from All Databases)

Important Invention Disclosures for the Duration of the Center's Operation

Summary patent filings for MIND

Non-majority MQCA Magnetic Logic Gates and Arrays based on Misaligned Magnetic Islands
Inventors: Mike Niemier, Gary Bernstein, Wolfgang Porod
Patent no. US 8,058,906
Issued November 2011

Tunneling Field-Effect Transistor with Low Leakage Current
Inventors: Mathieu Luisier, Samarth Agarwal, Gerhard Klimeck
Patent no. US 8,309,989 B2
Issued November 2012

Improved Lateral g-FET Design
Inventors: Gerhard Klimeck
Utility patent filed September 2010

Low Voltage Tunnel Field-Effect Transistor (TFET) and Method of Making Same
Inventors: Alan Seabaugh, Patrick Fay, Huili Xing, Yeqing Lu, Guangle Zhou, Mark Wistey, Siyuranga Koswatta
Utility patent filed August 2011

Method and Apparatus for Terahertz Wave Amplitude Modulation
Inventors: Berardi Sensale-Rodriguez, Rusen Yan, Michelle Kelly, Tian Fang, Debdeep Jena, Lei Liu, Huili Xing
Utility patent filed June 2012

Summary invention disclosures pending

Structure and Process for Multiple-Conductor Wrap-Around-Gate Field Effect Transistors with Channel Dimensions Set by Epitaxial Growth
Inventors: Mark Wistey, Mark Rodwell, Yaacov Doron, Cohen Elias, Andrew Carter
Disclosure filed June 2012 – transferred to Nonclassical CMOS Center

Single Transistor Random Access Memory Using Ion Storage In 2D Crystals
Inventors: Alan Seabaugh, Susan Fullerton
Disclosure filed September 2012